EXC-1394PCI
&
EXC-1394PCIe

Test and Simulation Boards for PCI Systems

User's Manual

EXCALIBUR SYSTEMS

311 Meacham Avenue ♦ Elmont, N.Y. 11003 ♦ Tel. (516) 327-000 ♦ Fax (516) 327-4645
e-mail: excalibur@mil-1553.com website: www.mil-1553.com

Copyright © 2008 – 2015 Excalibur Systems. All Rights Reserved.

Table of Contents

Chapter 1 Introduction

1.1 Overview 1-1
- 1.1.1 Board Features 1-2
- 1.1.2 Block Diagram 1-4

1.2 Installation 1-5
- 1.2.1 Installing the Board 1-5
- 1.2.2 Installing Excalibur Software Tools 1-6

1.3 Technical Support 1-6

Chapter 2 PCI Architecture

2.1 PCI Memory Structure 2-2

2.2 PCI Configuration Space Header 2-2

2.3 PCI Configuration Registers 2-4
- 2.3.1 Vendor Identification Register (VID) 2-4
- 2.3.2 Device Identification Register (DID) for PCI 2-4
- 2.3.3 PCI Command Register (PCICMD) 2-4
- 2.3.4 PCI Status Register (PCISTS) 2-5
- 2.3.5 Revision Identification Register (RID) 2-6
- 2.3.6 Class Code Register (CLCD) 2-6
- 2.3.7 Cache Line Register Size Register (CALN) 2-7
- 2.3.8 Latency Timer Register (LAT) 2-7
- 2.3.9 Header Type Register (HDR). 2-7
- 2.3.10 Built-In Self-Test Register (BIST) 2-7
- 2.3.11 Base Address Registers (BADR) 2-7
- 2.3.12 Cardbus CIS Pointer 2-9
- 2.3.13 Subsystem ID 2-9
- 2.3.14 Subvendor ID 2-9
- 2.3.15 Expansion ROM Base Address Register (XROM) 2-9
- 2.3.16 PCI Capabilities Pointer 2-9
- 2.3.17 Interrupt Line Register (INTLN) 2-9
- 2.3.18 Interrupt Pin Register (INTPIN) 2-10
- 2.3.19 Minimum Grant Register (MINGNT) 2-10
- 2.3.20 Maximum Latency Register (MAXLAT) 2-10

2.4 DMA Registers (for PCI Express) 2-10
- 2.4.1 DMA0 Address of Contiguous Host Memory 2-11
- 2.4.2 DMA0 Data Transfer Size 2-11
- 2.4.3 DMA0 Control Register 2-12
- 2.4.4 DMA1 Address of Contiguous Host Memory 2-12
- 2.4.5 DMA1 Data Transfer Size 2-13
- 2.4.6 DMA1 Control Register 2-13
- 2.4.7 DMA Interrupt Status Register 2-14
- 2.4.8 Base Address for DMA0 and DMA1 Transfers 2-14

2.5 Node Memory Space Map 2-14

2.6 Global Registers Map 2-15
- 2.6.1 Board Identification Register 2-16
- 2.6.2 Software Reset Register 2-16
- 2.6.3 Interrupt Status Register 2-16
- 2.6.4 Interrupt Reset Register 2-17
- 2.6.5 Node Info Registers 2-17

2.6.6 Time Tag Clock Select Register 2-18

2.7 IRIG B Global Registers 2-19

2.7.1 Sync IRIG B Register 2-20
2.7.2 IRIG B Time SBS High Register 2-20
2.7.3 IRIG B Time SBS Low Register 2-20
2.7.4 IRIG B Time Days Register 2-21
2.7.5 IRIG B Time Hours Register 2-21
2.7.6 IRIG B Time Minutes Register 2-21
2.7.7 IRIG B Time Seconds Register 2-21
2.7.8 Control Functions High and Low Registers 2-21
2.7.9 FPGA Revision Register 2-21

2.8 Global Timer Registers 2-22

2.8.1 Timer Prescale Register 2-22
2.8.2 Timer Preload Register 2-22
2.8.3 Timer Control Register 2-23
2.8.4 General Purpose Timer Register 2-23

Chapter 3 Node Operation Overview

3.1 Node General Memory Map 3-1

Chapter 4 Control Computer Operation

4.1 CC Memory Map 4-2

4.2 CC Mode Register Definitions 4-4

4.2.1 Hardware Revision Register 4-4
4.2.2 Excalibur Node ID Register 4-4
4.2.3 Interrupt Status Register 4-4
4.2.4 Interrupt Mask Register 4-5
4.2.5 Reset Time Register 4-6
4.2.6 Time Tag Registers 4-6
4.2.7 Reset Node Register 4-7
4.2.8 Vehicle Time Preload Value Register 4-7
4.2.9 Transmit Message Counter Register 4-7
4.2.10 Receive Message Counter Register 4-8
4.2.11 STOF Message Counter Register 4-8
4.2.12 Receive Message Error Counter Register 4-8
4.2.13 Transmit Message Error Counter Register 4-8
4.2.14 Discarded Message Counter Register 4-9
4.2.15 Firmware Revision Register 4-9
4.2.16 Pointer to Current Entry of Transmit Stack 4-9
4.2.17 Mode Select Register 4-9
4.2.18 Start Register 4-10
4.2.19 Excalibur Node Status Register 4-10
4.2.20 Port Status Register 4-11
4.2.21 1394 Node ID Register 4-13
4.2.22 CC Run Configuration Register 4-13
4.2.23 Pointer to Beginning of Single-Shot Stack 4-13
4.2.24 Pointer to Beginning of Continuous Mode Stack 4-14
4.2.25 Pointer to Beginning of Receive Linked List 4-14
4.2.26 Pointer to End of Receive Linked List 4-14
4.2.27 Speed Code Register 4-14
4.2.28 Options Register 4-15
4.2.29 STOF Period Register 4-15
4.2.30 Last STOF Message Status Register 4-15
4.2.31 Last STOF Message Area 4-16
4.2.32 Last STOF Time Tag Registers 4-16
4.2.33 Pointer to Most Recent Message 4-17

4.2.34 Pointer to Least Recent Message 4-17
4.2.35 Message Type Receive Control Table 4-17
4.2.36 CC STOF Offsets Table 4-18

4.3 Message Area 4-18

4.3.1 CC Transmit Messages 4-18
4.3.2 CC Transmit Stacks 4-19
4.3.3 CC Linked List Area 4-21

Chapter 5 Remote Node Operation

5.1 RN Memory Map 5-2

5.2 RN Mode Register Definitions 5-4

5.2.1 Hardware Revision Register 5-4
5.2.2 Excalibur Node ID Register 5-4
5.2.3 Interrupt Status Register 5-4
5.2.4 Interrupt Mask Register 5-5
5.2.5 Reset Time Register 5-6
5.2.6 Time Tag Registers 5-6
5.2.7 Reset Node Register 5-6
5.2.8 Transmit Message Counter Register 5-7
5.2.9 Receive Message Counter Register 5-7
5.2.10 STOF Message Counter Register 5-7
5.2.11 Receive Message Error Counter Register 5-7
5.2.12 Transmit Message Error Counter Register 5-8
5.2.13 Discarded Message Counter Register 5-8
5.2.14 Firmware Revision Register 5-8
5.2.15 Pointer to Current Entry of Transmit Stack 5-8
5.2.16 Mode Select Register 5-9
5.2.17 Start Register 5-9
5.2.18 Excalibur Node Status Register 5-9
5.2.19 Port Status Register 5-10
5.2.20 Number of Bad STOF Messages for CC Fail Register 5-12
5.2.21 1394 Node ID Register 5-12
5.2.22 Pointer to Beginning of Transmit Stack 5-12
5.2.23 Pointer to Beginning of Datapump Stack 5-12
5.2.24 Pointer to Beginning of Receive Stack 5-12
5.2.25 Pointer to End of Receive Stack 5-13
5.2.26 Speed Code Register 5-13
5.2.27 Options Register 5-13
5.2.28 STOF Period Register 5-14
5.2.29 Last STOF Message Status Register 5-14
5.2.30 Last STOF Message Area 5-15
5.2.31 Last STOF Time Tag Registers 5-15
5.2.32 Store STOF Messages Register 5-15
5.2.33 Receive STOF Offset Register 5-16
5.2.34 Transmit STOF Offset Register 5-16
5.2.35 Datapump STOF Offset Register 5-17
5.2.36 Channel Number Register 5-17
5.2.37 Receive STOF Offset In Use Register 5-17
5.2.38 Transmit STOF Offset In Use Register 5-18
5.2.39 Datapump STOF Offset In Use Register 5-18
5.2.40 Message Type Receive Control Table 5-18

5.3 Message Area 5-19

5.3.1 RN Transmit/Datapump Messages 5-19
5.3.2 RN Transmit/Datapump Message Stacks 5-20
5.3.3 RN Receive Message Stack 5-22
5.3.4 RN Receive Data Blocks 5-23

Chapter 6 Asynchronous Operation

6.1 Asynchronous Memory Map 6-2

6.2 Asynchronous Mode Register Definitions 6-3

6.2.1 Hardware Revision Register 6-3
6.2.2 Excalibur Node ID Register 6-3
6.2.3 Interrupt Status Register 6-3
6.2.4 Interrupt Mask Register 6-4
6.2.5 Reset Time Register 6-5
6.2.6 Time Tag Registers 6-5
6.2.7 Receive Message Counter Register 6-5
6.2.8 Receive Message Error Counter Register 6-6
6.2.9 Discarded Message Counter Register 6-6
6.2.10 Firmware Revision Register 6-6
6.2.11 Mode Select Register 6-6
6.2.12 Start Register 6-7
6.2.13 Excalibur Node Status Register 6-7
6.2.14 Port Status Register 6-9
6.2.15 Options Register 6-10

6.3 Message Area 6-11

6.3.1 Asynchronous Transmit Message Areas 6-11
6.3.2 Asynchronous Receive Message Area 6-14

Chapter 7 Bus Monitor Operation

7.1 Bus Monitor Memory Map 7-2

7.2 Bus Monitor Mode Register Definitions 7-4

7.2.1 Hardware Revision Register 7-4
7.2.2 Excalibur Node ID Register 7-4
7.2.3 Interrupt Status Register 7-4
7.2.4 Interrupt Mask Register 7-5
7.2.5 Reset Time Register 7-6
7.2.6 Time Tag Registers 7-7
7.2.7 Reset Node Register 7-7
7.2.8 Receive Message Counter Register 7-7
7.2.9 STOF Message Counter Register 7-8
7.2.10 Receive Message Error Counter Register 7-8
7.2.11 Discarded Message Counter Register 7-8
7.2.12 Firmware Revision Register 7-8
7.2.13 Mode Select Register 7-9
7.2.14 Start Register 7-9
7.2.15 Excalibur Node Status Register 7-9
7.2.16 Port Status Register 7-10
7.2.17 Number of Bad STOF Messages for CC Fail Register 7-12
7.2.18 Pointer to Beginning of Receive Linked List 7-12
7.2.19 Pointer to Beginning of Receive Stack 7-12
7.2.20 Pointer to End of Receive Stack 7-12
7.2.21 Options Register 7-13
7.2.22 STOF Period Register 7-13
7.2.23 Last STOF Message Status Register 7-13
7.2.24 Last STOF Message Area 7-14
7.2.25 Last STOF Time Tag Registers 7-15
7.2.26 Store STOF Messages Register 7-15
7.2.27 Pointer to Most Recent Message 7-15
7.2.28 Pointer to Least Recent Message 7-16
7.2.29 Pointer to Trigger Message 7-16
7.2.30 Trigger Control Register 7-16
7.2.31 Trigger Position Register 7-17

7.2.32 Linked List Fill Control Register ... 7-18
7.2.33 Control Table Selection Register ... 7-18
7.2.34 STOF Offsets Control Register ... 7-18
7.2.35 STOF Filter Window Begin Register ... 7-19
7.2.36 STOF Filter Window End Register ... 7-19
7.2.37 Memory Select Register ... 7-20
7.2.38 Bank Select Register ... 7-20
7.2.39 Current Bank Register ... 7-21
7.2.40 PHY Base Registers ... 7-21
7.2.41 PHY Port 0 Status Registers ... 7-21
7.2.42 PHY Port 1 Status Registers ... 7-21
7.2.43 PHY Port 2 Status Registers ... 7-22
7.2.44 Monitor Control Tables ... 7-22
7.2.45 Bus Monitor STOF Offsets Table ... 7-23
7.2.46 Data Trigger Table ... 7-24

7.3 Message Area ... 7-26

7.3.1 Bus Monitor Receive Stack ... 7-26
7.3.2 Bus Monitor Linked List ... 7-27
7.3.3 Banked Window into SDRAM ... 7-31

Chapter 8 Mechanical and Electrical Specifications

8.1 Board Layout ... 8-1

8.2 LED Indicators ... 8-2

8.3 DIP Switches ... 8-3

8.3.1 Selected ID DIP Switch [SW1] ... 8-3

8.4 Connectors ... 8-4

8.4.1 Communications I/O Connector [J1] ... 8-4
8.4.2 PCI Bus Edge Connector Pinouts ... 8-8
8.4.3 PCI Express Bus Edge Connector Pinouts ... 8-10

8.5 Synchronization with External Sources ... 8-11

8.6 Synchronizing Between EXC-1394PCI[e] Boards ... 8-12

8.7 Power Requirements ... 8-12

Chapter 9 Ordering Information

Appendix A 1394 Message Formats

Figures

Figure 1-1: *EXC-1394PCI* Block Diagram 1-4
Figure 1-2: *EXC-1394PCIe* Block Diagram 1-5
Figure 2-1: PCI Configuration Space Header (for PCI) 2-3
Figure 2-2: PCI Configuration Space Header (for PCI Express) 2-3
Figure 2-3: DMA Registers Map 2-11
Figure 2-4: Node Memory Space Map 2-14
Figure 2-5: *EXC-1394PCI[e]* Global and IRIG B Registers Map 2-15
Figure 4-1: Transmit Message 4-19
Figure 5-1: Transmit Message 5-20
Figure 5-2: RN Receive Data Block 5-23
Figure 6-1: Asynchronous [Stream] Transmit Message 6-13
Figure 6-2: Asynchronous Receive Message 6-15
Figure 8-1: *EXC-1394PCI* Board Layout 8-1
Figure 8-2: *EXC-1394PCIe* Board Layout 8-2
Figure 8-3: DIP Switch SW1 with All Switches Set to ON (Select ID#0) 8-3
Figure 8-4: Connectors J1 Layout – Front View 8-4
Figure 8-5: Synchronization of an *EXC-1394PCI[e]* Board to an External System 8-11
Figure 8-6: Synchronization of an External System to an *EXC-1394PCI[e]* Board 8-11
Figure 8-7: Synchronization Between *EXC-1394PCI[e]* Boards 8-12
Figure A-1: STOF Packet Format A-1
Figure A-2: Asychronous Data Packet Format A-2

Tables

Table 2-1: PCI Command Register 2-4
Table 2-2: PCI Status Register (for PCI) 2-5
Table 2-3: PCI Status Register (for PCI Express) 2-6
Table 2-4: Base Address Registers Definition for PCI 2-8
Table 2-5: Base Address Registers Definition for PCI Express 2-8
Table 2-6: Base Address Register for PCI 2-8
Table 2-7: Base Address Register for PCI Express 2-8
Table 2-8: DMA0 Control Register 2-12
Table 2-9: DMA1 Control Register 2-13
Table 2-10: Board Identification Register 2-16
Table 2-11: Software Reset Register 2-16
Table 2-12: Interrupt Status Register 2-17
Table 2-13: Interrupt Reset Register 2-17
Table 2-14: Node Info Registers 2-18
Table 2-15: Time Tag Clock Select Register 2-18
Table 2-16: Sync IRIG B Register 2-20
Table 2-17: Timer Prescale/General Purpose Timer Resolution 2-22
Table 2-18: Timer Control Register 2-23

Table 3-1: Node General Memory Map 3-1
Table 4-1: CC Mode Memory Map Registers 4-2
Table 4-2: Interrupt Status Register 4-5
Table 4-3: Interrupt Mask Register 4-6
Table 4-4: Reset Time Register 4-6
Table 4-5: Time Tag Registers 4-7
Table 4-6: Reset Node Register 4-7
Table 4-7: Vehicle Time Preload Value 4-7
Table 4-8: Transmit Message Counter Register 4-7
Table 4-9: Receive Message Counter Register 4-8
Table 4-10: STOF Message Counter Register 4-8
Table 4-11: Receive Message Error Counter Register 4-8
Table 4-12: Transmit Message Error Counter Register 4-9
Table 4-13: Discarded Message Counter Register 4-9
Table 4-14: Mode Select Register 4-10
Table 4-15: Start Register 4-10
Table 4-16: Excalibur Node Status Register 4-11
Table 4-17: Port Status Register 4-12
Table 4-18: Port Speed Bits 4-12
Table 4-19: 1394 Node ID 4-13
Table 4-20: CC Run Configuration Register 4-13
Table 4-21: Speed Code Register 4-14
Table 4-22: Speed Code Bits 4-14
Table 4-23: Options Register 4-15
Table 4-24: STOF Period Register 4-15
Table 4-25: Last STOF Message Status Register 4-16
Table 4-26: Last STOF Message Area 4-16
Table 4-27: Last STOF Time Tag Registers 4-16
Table 4-28: Pointer to Most Recent Message 4-17
Table 4-29: Pointer to Least Recent Message 4-17
Table 4-30: CC Receive Control Word 4-17
Table 4-31: CC STOF Offsets Table 4-18
Table 4-32: Transmit Message Data Area 4-18
Table 4-33: CC Transmit Stack Entry 4-20
Table 4-34: CC Transmit Stack Control Word 4-20
Table 4-35: CC Transmit Stack Status Word 4-20
Table 4-36: CC Linked List Structure 4-21
Table 4-37: CC Receive Message Status Word 4-22
Table 5-1: RN Mode Memory Map Registers 5-2
Table 5-2: Interrupt Status Register 5-5
Table 5-3: Interrupt Mask Register 5-5
Table 5-4: Reset Time Register 5-6
Table 5-5: Time Tag Registers 5-6
Table 5-6: Reset Node Register 5-6
Table 5-7: Transmit Message Counter Register 5-7

Table 5-8: Receive Message Counter Register 5-7
Table 5-9: STOF Message Counter Register 5-7
Table 5-10: Receive Message Error Counter Register 5-8
Table 5-11: Transmit Message Error Counter Register 5-8
Table 5-12: Discarded Message Counter Register 5-8
Table 5-13: Mode Select Register 5-9
Table 5-14: Start Register 5-9
Table 5-15: Excalibur Node Status Register 5-10
Table 5-16: Port Status Register 5-11
Table 5-17: Port Speed Bits 5-11
Table 5-18: Number of Bad STOF Messages for CC Fail Register 5-12
Table 5-19: 1394 Node ID Register 5-12
Table 5-20: Speed Code Register 5-13
Table 5-21: Speed Code Bits 5-13
Table 5-22: Options Register 5-13
Table 5-23: STOF Period Register 5-14
Table 5-24: Last STOF Message Status Register 5-14
Table 5-25: Last STOF Message Area 5-15
Table 5-26: Last STOF Time Tag Registers 5-15
Table 5-27: Store STOF Messages Register 5-16
Table 5-28: Receive STOF Offset Register 5-16
Table 5-29: Transmit STOF Offset Register 5-16
Table 5-30: Datapump STOF Offset Register 5-17
Table 5-31: Channel Number Register 5-17
Table 5-32: Receive STOF Offset In Use Register 5-17
Table 5-33: Transmit STOF Offset In Use Register 5-18
Table 5-34: Datapump STOF Offset In Use Register 5-18
Table 5-35: Message Type Receive Control Table 5-18
Table 5-36: Control Word 5-19
Table 5-37: RN Message Data Area 5-19
Table 5-38: RN Transmit/Datapump Stack Entry 5-21
Table 5-39: RN Transmit Stack Entry Control Word 5-21
Table 5-40: RN Transmit Stack Entry Status Word 5-21
Table 5-41: RN Receive Message Stack 5-22
Table 5-42: RN Receive Message Stack Status Word 5-22
Table 5-43: Data Block Header 5-25
Table 5-44: Data Block Header Control Word 5-25
Table 5-45: Buffer Size Bits 5-25
Table 5-46: Data Block Header Status Word 5-26
Table 5-47: Data Block Buffer 5-26
Table 5-48: Buffer Status Word 5-27
Table 6-1: RN Mode Memory Map Registers 6-2
Table 6-2: Interrupt Status Register 6-4
Table 6-3: Interrupt Mask Register 6-4
Table 6-4: Reset Time Register 6-5

Table 6-5: Time Tag Registers 6-5
Table 6-6: Receive Message Counter Register 6-5
Table 6-7: Receive Message Error Counter Register 6-6
Table 6-8: Discarded Message Counter Register 6-6
Table 6-9: Mode Select Register 6-7
Table 6-10: Start Register 6-7
Table 6-11: Excalibur Node Status Register 6-8
Table 6-12: Port Status Register 6-9
Table 6-13: Port Speed Bits 6-9
Table 6-14: Options Register 6-10
Table 6-15: Transmit Handshake Registers 6-12
Table 6-16: Control Word Bits 6-12
Table 6-17: Status Word Bits 6-12
Table 6-18: Ack Codes 6-13
Table 6-19: 1394 Header and Data Area 6-13
Table 6-20: Receive Message Information Registers 6-14
Table 6-21: Status Word Bits 6-14
Table 6-22: 1394 Header and Data Area 6-15
Table 7-1: Bus Monitor Mode Memory Map Registers 7-2
Table 7-2: Interrupt Status Register 7-5
Table 7-3: Interrupt Mask Register 7-6
Table 7-4: Reset Time Register 7-6
Table 7-5: Time Tag Registers 7-7
Table 7-6: Reset Node Register 7-7
Table 7-7: Receive Message Counter Register 7-7
Table 7-8: STOF Message Counter Register 7-8
Table 7-9: Receive Message Error Counter Register 7-8
Table 7-10: Discarded Message Counter Register 7-8
Table 7-11: Mode Select Register 7-9
Table 7-12: Start Register 7-9
Table 7-13: Excalibur Node Status Register 7-10
Table 7-14: Port Status Register 7-11
Table 7-15: Port Speed Bits 7-11
Table 7-16: Number of Bad STOF Messages for CC Fail Register 7-12
Table 7-17: Options Register 7-13
Table 7-18: STOF Period Register 7-13
Table 7-19: Last STOF Message Status Register 7-14
Table 7-20: Last STOF Message Area 7-14
Table 7-21: Last STOF Time Tag Registers 7-15
Table 7-22: Store STOF Messages Register 7-15
Table 7-23: Pointer to Most Recent Message 7-15
Table 7-24: Pointer to Least Recent Message 7-16
Table 7-25: Pointer to Trigger Message 7-16
Table 7-26: Trigger Control Register 7-17
Table 7-27: Trigger Position Register 7-17

Table 7-28: Linked List Fill Control Register 7-18
Table 7-29: Control Table Selection Register 7-18
Table 7-30: STOF Offsets Control Register 7-19
Table 7-31: STOF Filter Window Begin Register 7-19
Table 7-32: STOF Filter Window End 7-19
Table 7-33: Memory Select Register 7-20
Table 7-34: Bank Select Register 7-20
Table 7-35: Current Bank Register 7-21
Table 7-36: Monitor Mode Receive Control Table 7-22
Table 7-37: Bus Monitor STOF Offsets Table 7-23
Table 7-38: Bus Monitor STOF Offsets Table Control Word 7-24
Table 7-39: Bus Monitor STOF Offsets Table Status Word 7-24
Table 7-40: Bus Monitor Data Trigger Table 7-25
Table 7-41: Bus Monitor Data Trigger Control Word 7-25
Table 7-42: Bus Monitor Data Trigger Status Word 7-25
Table 7-43: Bus Monitor Receive Stack 7-26
Table 7-44: Bus Monitor Message Stack Status Word 7-27
Table 7-45: Bus Monitor Linked List Structure for a General Message 7-28
Table 7-46: Receive Message Status Word for a General Message 7-29
Table 7-47: Bus Monitor Linked List Structure for a STOF Message 7-30
Table 7-48: Receive Message Status Word for a STOF Message 7-31
Table 8-1: LED Indicators 8-2
Table 8-2: Dip Switch Settings for Unique ‘Selected ID’ 8-3
Table 8-3: Selected ID Bits 8-3
Table 8-4: J1 Connector Pinouts 8-5
Table 8-5: J1 Connector Signal Descriptions 8-6
Table 8-6: PCI Bus Edge Connector Pinouts 8-8
Table 8-7: PCI Express Bus Edge Connector Pinouts 8-10
Table 9-1: Ordering Information 9-1

Chapter 1 Introduction

Chapter 1 provides an overview of the *EXC-1394PCI* and *EXC-1394PCIe* avionics communication boards. The following topics are covered:

1.1 Overview 1-1
1.1.1 Board Features 1-2
1.1.2 Block Diagram 1-4
1.2 Installation 1-5
1.2.1 Installing the Board 1-5
1.2.2 Installing Excalibur Software Tools 1-6
1.3 Technical Support 1-6

1.1 Overview

The *EXC-1394PCI[e]* is an intelligent test and simulation board for interfacing with an IEEE-1394 data bus. It implements a 1394b physical layer, which can operate at 100, 200, or 400 Mbps. It provides up to three fully independent nodes (each node having three full-duplex ports associated with it) and has a universal PCI interface that is compatible with any 32-bit, 33/66 MHz PCI slot. It interfaces with the 1394 bus through a high density 62-pin DB type female connector. The board comes with onboard active transformers.

Each node has 2 MB of memory for message data and control registers. A 48-bit Time Tag is used to provide accurate time stamping of messages. All STOF offsets are programmable, as is the STOF timing (frame rate) itself.

Each node can operate in one of the following modes:

- Control Computer (CC) mode
- Remote Node (RN) mode
- Bus Monitor mode
- Asynchronous mode

CC mode – In CC mode, the node acts as the Root Node and Bus Manager, and is responsible for sending out the STOF message at a precise, predefined, programmable interval. It has two Transmit Stacks, one for Single-Shot and one for Continuous, to allow the first frame to be configured differently than the other frames. The node has programmable STOF offsets for each RN with two receive offsets for each RN: one for the Single-Shot Stack and one for the Continuous Stack. Receive messages can be filtered by a combination of message number and transmitting RN (message type). Interrupts can be requested for all messages or for specific message types, as well as for various error conditions.

RN mode – In RN mode, the node acts as a remote node on the Bus. It transmits according to its predefined transmit STOF offset and has separate stacks for transmitting regular messages and Datapump messages. It is ready to receive data at any time during the STOF frame. Received data can be filtered by a combination of message number and transmitting RN (message type). Data blocks are configurable for each message type, with up to eight buffers per data block and a

selectable buffer size. Interrupts can be requested for all messages or for specific data buffers, as well as various error conditions.

Bus Monitor mode – In Bus Monitor mode, the node receives all bus messages that pass through its ports, and stores them in memory with their timestamps. Filtering is available for storing only specific messages. Triggering is available to capture a snapshot of data surrounding a specific event. Data can be recorded either to the almost 2-MB Dual Port RAM buffer or to a 128-MB SDRAM buffer. The Dual Port RAM can be used for real time monitoring. The 128-MB SDRAM should be used in conjunction with triggering to record a large buffer relating to a specific event. 1 MB at a time can be accessed via DPRAM when the node is stopped.

Asynchronous mode – Asynchronous mode is a simple command-response mode. In this mode, after sending a message, the node will not send another message until a response is received or the timeout period defined in the message has passed. The one exception is an Asynchronous Stream message. When sending an Asynchronous Stream message, the node does not wait for a response and another message can be transmitted immediately.

Note: Startup and Initializing modes are not supported.

1.1.1 Board Features

General Features

- Supports up to three IEEE-1394 nodes, with three ports per node
- IEEE-1394b PHY
- Operating modes: CC, RN, Asynchronous or Bus Monitor
- Supports AS5643
- Autonomous operation in all modes
- 2 MB dual-port RAM per node
- 128 MB SDRAM per node
- 48 bit Time Tag
- Polling or interrupt driven
- Real-time operation
- Programmable STOF offsets
- Flexible interrupt support
- Receive message filtering

Control Computer

- Support for unique initial frame (for changing STOF offsets)
- Single-Shot and Continuous stacks
- Two receive offsets for each node
- Error injection:

  1394 header error

  ASM header error

  Footer quadlet error

Remote Node

- Transmits at predefined STOF offsets
- Receives data any time during the STOF frame
- Multiple receive buffers (up to eight)
- STOF error detection
- Configurable data blocks

Bus Monitor

- Real-time monitoring with 2 MB dual-port RAM
- 128 MB buffer for later analysis
- STOF error detection
- Several triggering options for capturing current bus data

Physical Characteristics

- Dimensions: 157.0 mm x 107.0 mm
- Weight: 140 grams

Operation Environment

- Temperature:

  0° to +70°C

  -40° to +85°C (optional)

- Humidity: 5%–90% noncondensing
- MTBF:

  For PCI: 73,830 hours at 25°C, G_F, S217F

  For PCI Express: 70,480 hours at 25°C, G_F, S217F

Host Interface

- PCI/PCIe compliance:

  For PCI: Master/Target 16/32 bit, 33 MHz clock speed

  For PCI Express: x1 lane PCIe v1.1

- Memory space occupied: 8 MB
- Interrupts:

  For PCI: INTA#

  For PCI Express: INTA# Virtual Wire

- Power:

  For PCI: 1.8A @ 5V

  For PCI Express: 2.1A @ 3.3V

Software Support

- C drivers with source code
- *Exalt Plus:* Excalibur Analysis Laboratory Tools (optional)

See Ordering Information on page 9-1, for the exact part numbers.

1.1.2 Block Diagram

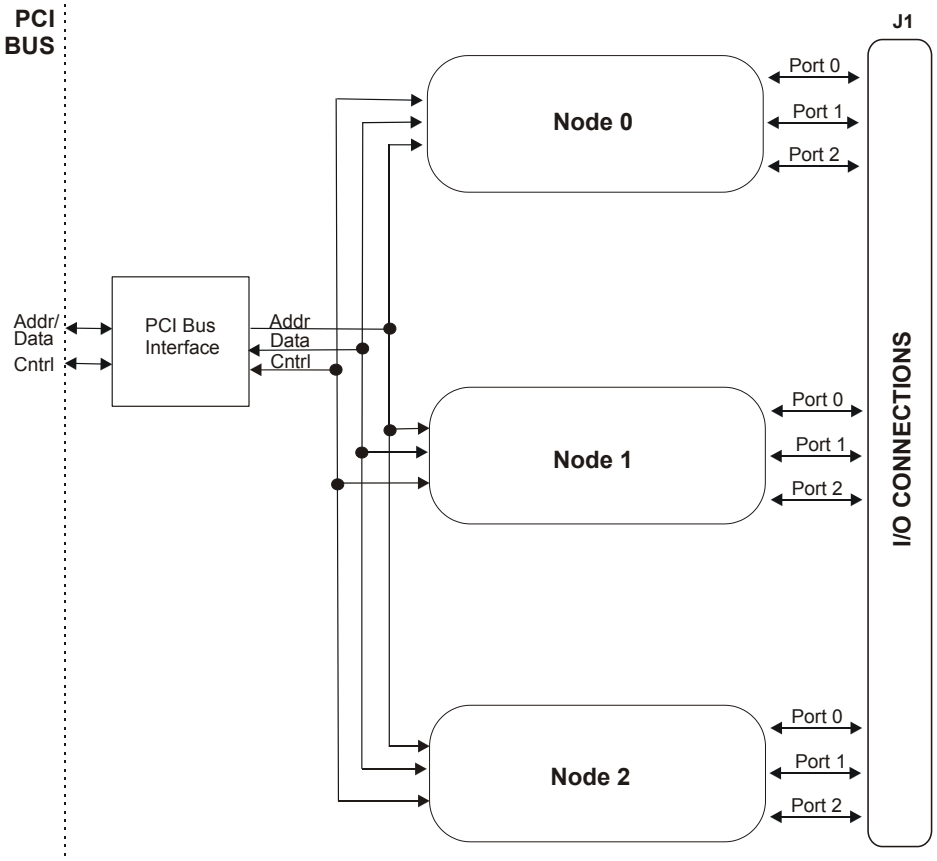

Figure 1-1: ***EXC-1394PCI*** **Block Diagram**

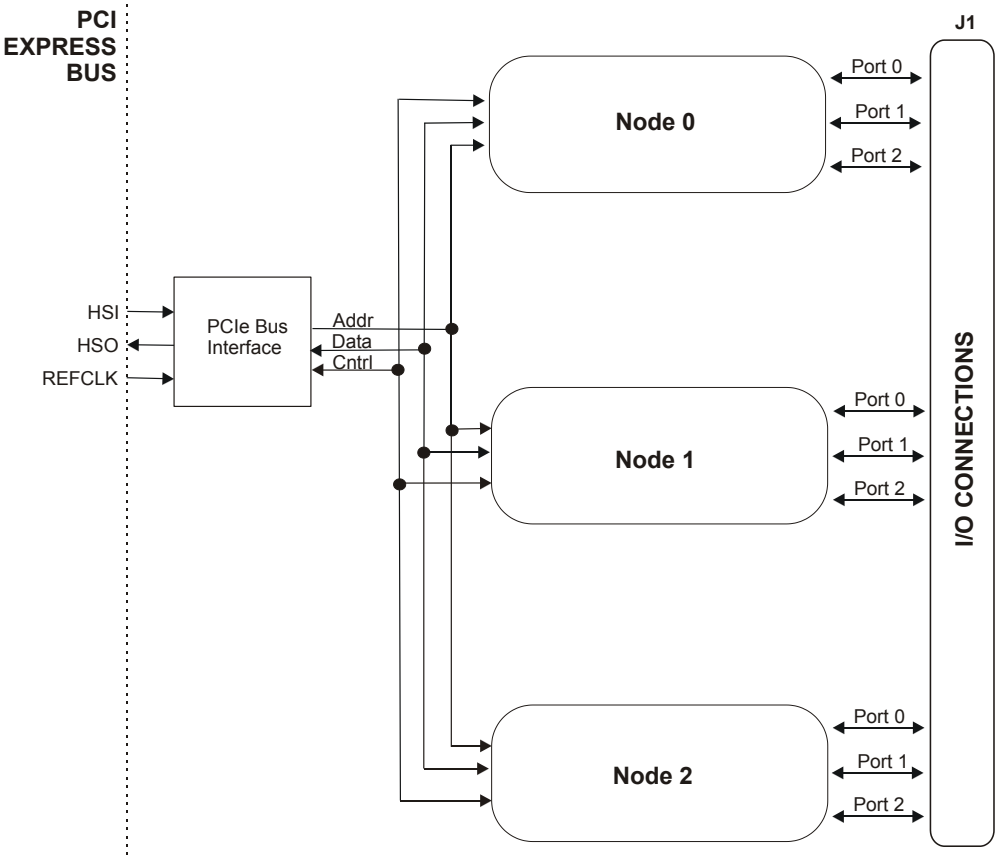

Figure 1-2: *EXC-1394PCIe* Block Diagram

1.2 Installation

To operate the *EXC-1394PCI[e]* board:

- Install the board in your computer.
- Install the *Software Tools*.

1.2.1 Installing the Board

Installation of the *EXC-1394PCI[e]* board is similar to that of all PCI "Local Bus" boards. The *EXC-1394PCI[e]* complies with the "Plug and Play" specification of the PCI standard. Therefore, its absolute address is determined by the BIOS at start-up.

Caution: *Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board and use all necessary antistatic precautionary measures.*

To install the *EXC-1394PCI[e]*:

1. Make sure that the computer power source is disconnected.
2. Insert the *EXC-1394PCI[e]* board into any PCI slot.
3. Tighten the *EXC-1394PCI[e]* board's PCI bracket with the slot screw to ground the board to the computer.

4. Attach the adapter cable to the board and to the communication bus. The cable may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting over the bus.

1.2.2 Installing Excalibur Software Tools

For hardware and software installation instructions, see the readme.pdf file on the root folder of the installation CD. When downloading new software from the Excalibur website, the readme.pdf file is contained in the zip file.

The Excalibur Installation CD you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.3 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, see the Technical Support section of our website: www.mil-1553.com. You can also contact us by phone. To find the location nearest you, see the Contact section of our website.

Chapter 2 PCI Architecture

Chapter 2 describes the PCI architecture. The following topics are covered:

2.1 PCI Memory Structure 2-2

2.2 PCI Configuration Space Header 2-2

2.3 PCI Configuration Registers 2-4

2.3.1 Vendor Identification Register (VID) 2-4
2.3.2 Device Identification Register (DID) for PCI 2-4
2.3.3 PCI Command Register (PCICMD) 2-4
2.3.4 PCI Status Register (PCISTS) 2-5
2.3.5 Revision Identification Register (RID) 2-6
2.3.6 Class Code Register (CLCD) 2-6
2.3.7 Cache Line Register Size Register (CALN) 2-7
2.3.8 Latency Timer Register (LAT) 2-7
2.3.9 Header Type Register (HDR). 2-7
2.3.10 Built-In Self-Test Register (BIST) 2-7
2.3.11 Base Address Registers (BADR) 2-7
2.3.12 Cardbus CIS Pointer 2-9
2.3.13 Subsystem ID 2-9
2.3.14 Subvendor ID 2-9
2.3.15 Expansion ROM Base Address Register (XROM) 2-9
2.3.16 PCI Capabilities Pointer 2-9
2.3.17 Interrupt Line Register (INTLN) 2-9
2.3.18 Interrupt Pin Register (INTPIN) 2-10
2.3.19 Minimum Grant Register (MINGNT) 2-10
2.3.20 Maximum Latency Register (MAXLAT) 2-10

2.4 DMA Registers (for PCI Express) 2-10

2.4.1 DMA0 Address of Contiguous Host Memory 2-11
2.4.2 DMA0 Data Transfer Size 2-11
2.4.3 DMA0 Control Register 2-12
2.4.4 DMA1 Address of Contiguous Host Memory 2-12
2.4.5 DMA1 Data Transfer Size 2-13
2.4.6 DMA1 Control Register 2-13
2.4.7 DMA Interrupt Status Register 2-14
2.4.8 Base Address for DMA0 and DMA1 Transfers 2-14

2.5 Node Memory Space Map 2-14

2.6 Global Registers Map 2-15

2.6.1 Board Identification Register 2-16
2.6.2 Software Reset Register 2-16
2.6.3 Interrupt Status Register 2-16
2.6.4 Interrupt Reset Register 2-17
2.6.5 Node Info Registers 2-17
2.6.6 Time Tag Clock Select Register 2-18

2.7 IRIG B Global Registers 2-19

2.7.1 Sync IRIG B Register 2-20
2.7.2 IRIG B Time SBS High Register 2-20
2.7.3 IRIG B Time SBS Low Register 2-20
2.7.4 IRIG B Time Days Register 2-21
2.7.5 IRIG B Time Hours Register 2-21
2.7.6 IRIG B Time Minutes Register 2-21
2.7.7 IRIG B Time Seconds Register 2-21
2.7.8 Control Functions High and Low Registers 2-21
2.7.9 FPGA Revision Register 2-21

2.8 Global Timer Registers 2-22
2.8.1 Timer Prescale Register 2-22
2.8.2 Timer Preload Register 2-22
2.8.3 Timer Control Register 2-23
2.8.4 General Purpose Timer Register 2-23

2.1 PCI Memory Structure

The *EXC-1394PCI* requests two memory blocks:

- The first memory block (Base 0) is 8 MB in size and contains the memory space for the nodes on the board. For more information, see Node Memory Space Map on page 2-14.
- The second memory block (Base 1) is 128 bytes in size and contains the Global Registers. For more information, see Global Registers Map on page 2-15.

The *EXC-1394PCIe* requests three memory blocks:

- The first memory block (Base 0) is 8 MB in size and contains the memory space for the nodes on the board. For more information, see Node Memory Space Map on page 2-14.
- The second memory block (Base 2) is 4 KB in size and contains the Global Registers. For more information, see Global Registers Map on page 2-15.
- The third memory block (Base 4) is 8 KB in size and contains the DMA Registers. For more information, see DMA Registers (for PCI Express) on page 2-10.

2.2 PCI Configuration Space Header

The *EXC-1394PCI* and *EXC-1394PCIe* include a PCI Configuration Space Header, as required by PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	003C (H)
Reserved				0038 (H)
Reserved			Cap. pointer	0034 (H)
Expansion ROM Base Address (not used)				0030 (H)
Subsystem ID		Subsystem Vendor ID		002C (H)
Cardbus CIS Pointer (not used)				0028 (H)
Base Address Register #5 – (not used)				0024 (H)
Base Address Register #4 – (not used)				0020 (H)
Base Address Register #3 – (not used)				001C (H)
Base Address Register #2 – (not used)				0018 (H)
Base Address Register #1 – Global Registers				0014 (H)
Base Address Register #0 – Node Memory Space				0010 (H)
BIST	Header Type = 0	Latency Timer	Cache Line Size	000C (H)
Class Code			Rev ID	0008 (H)
Status Register		Command Register		0004 (H)
Device ID		Vendor ID		0000 (H)
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-1: PCI Configuration Space Header (for PCI)

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	003C (H)
Reserved				0038 (H)
Reserved			Cap. pointer	0034 (H)
Expansion ROM Base Address (not used)				0030 (H)
Subsystem ID		Subsystem Vendor ID		002C (H)
Cardbus CIS Pointer (not used)				0028 (H)
Base Address Register #5 – (not used)				0024 (H)
Base Address Register #4 – DMA Registers				0020 (H)
Base Address Register #3 – (reserved)				001C (H)
Base Address Register #2 – Global Registers				0018 (H)
Base Address Register #1 – (reserved)				0014 (H)
Base Address Register #0 – Node Memory Space				0010 (H)
BIST	Header Type = 0	Latency Timer	Cache Line Size	000C (H)
Class Code			Rev ID	0008 (H)
Status Register		Command Register		0004 (H)
Device ID		Vendor ID		0000 (H)
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-2: PCI Configuration Space Header (for PCI Express)

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID)

Address: 0000 (H) Length: 16 bits

Read Only

This register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems. The value at power-up is 1405 (H).

2.3.2 Device Identification Register (DID) for PCI

Address: 0002 (H) Length: 16 bits

Read Only

This register contains the board's device identification number.

For PCI: The value at power-up is 1394 (H).

For PCI Express: The value at power-up is EF00 (H).

2.3.3 PCI Command Register (PCICMD)

Address: 0004 (H) Length: 16 bits

Read Only

This register contains the PCI Command.

Table 2-1: PCI Command Register

Bit	Bit Name	Description
10 – 15	Reserved	Set to 0s
09	Fast Back to Back Enable	Always set to 0
08	System Error Enable	Always set to 0
07	Address Stepping Support	**For PCI:** Always set to 1 **For PCI Express:** Always set to 0
06	Parity Error Enable	Always set to 0
05	VGA Palette Snoop Enable	Always set to 0
04	Memory Write and Invalidate Enable	Always set to 0
03	Special Cycle Enable	Always set to 0
02	Bus Master Enable	**For PCI:** Always set to 0 **For PCI Express:** Always set to 1
01	Memory Access Enable	Always set to 1
00	I/O Access Enable	Since the *EXC-1394PCI[e]* board does not use I/O space, the value of this register is ignored.

2.3.4 PCI Status Register (PCISTS)

Address: 0006 (H) Length: 16 bits

Read Only

This register contains the PCI status information.

Table 2-2: PCI Status Register (for PCI)

Bit	Bit Name	Description
15	Detected Parity Error	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register, Bit 6. This bit may be cleared by writing a 1 to this location.
14	Signaled System Error	Not used
13	Received Master Abort	Not used
12	Received Target Abort	Not used
11	Signaled Target Abort	This bit is set whenever this device aborts a cycle when addressed as a target. This bit can be reset by writing a 1 to this location.
09 – 10	Device Select (DEVSEL#) Timing Status	Set to 10 (slow timing)
08	Data Parity Reported	Not used
07	Fast Back-to-Back Capable	Set to 1
06	Reserved	
05	66MHz capable	Set to 0
04	Capability List enable	Set to 1
00 – 03	Reserved	

Table 2-3: PCI Status Register (for PCI Express)

Bit	Bit Name	Description
15	Detected Parity Error	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register, Bit 6. This bit may be cleared by writing a 1 to this location.
14	Signaled System Error	Not used
13	Received Master Abort	This bit is set when the device receives a master abort to terminate a transaction. This bit can be reset by writing a 1 to this location.
12	Received Target Abort	Not used
11	Signaled Target Abort	Not used
09 – 10	Device Select (DEVSEL#) Timing Status	Set to 00 (fast timing)
08	Data Parity Reported	Not used
07	Fast Back-to-Back Capable	Set to 0
06	UDF Supported	Set to 0
05	66MHz capable	Set to 0
04	Capability List enable	Set to 1
03	Interrupt Status	This bit is set when an interrupt is received.
00 – 02	Reserved	

2.3.5 Revision Identification Register (RID)

Address: 0008 (H) Length: 8 bits

Read Only

This register contains the revision identification number of the *EXC-1394PCI[e]*. The value at power-up is 0001 (H).

2.3.6 Class Code Register (CLCD)

Address: 0009 (H) Length: 24 bits

Read Only

This register's value indicates that the *EXC-1394PCI[e]* does not fit into any of the defined class codes. The value at power-up is FF0000 (H).

2.3.7 Cache Line Register Size Register (CALN)

Address: 000C (H) Length: 8 bits

Read Only

For PCI: The value at power-up is 0000 (H).

For PCI Express: The value at power-up is 0010 (H).

Note: This register is not used on the *EXC-1394PCI[e]*.

2.3.8 Latency Timer Register (LAT)

Address: 000D (H) Length: 8 bits

The value at power-up is 0000 (H).

Note: This register is not used on the *EXC-1394PCI[e]*.

2.3.9 Header Type Register (HDR).

Address: 000E (H) Length: 8 bits

Read Only

This register contains whether the device is single or multifunction. The *EXC-1394PCI[e]* is a single function PCI device. Therefore, Bit 7 is set to '0'. The value at power-up is 0000 (H).

2.3.10 Built-In Self-Test Register (BIST)

Address: 000F (H) Length: 8 bits

Read Only

This register is not implemented in the *EXC-1394PCI[e]*. The value at power-up is 0000 (H).

2.3.11 Base Address Registers (BADR)

Address: 0010, 0014, 0018, 001C, 0020, 0024 (H) Length: 32 bits

Read Only

These registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space. The power-up value of each register is 0000 (H).

For PCI: Two memory pages are required by the board: one for the node memory space and one for the Global registers. See Table 2-4.

Table 2-4: Base Address Registers Definition for PCI

Register	Offset	Size	Function
Base Address 0	0010 (H)	8 MB	Node memory space
Base Address 1	0014 (H)	128 bytes	Global registers

For PCI Express: Three memory pages are required by the board: one for the node memory space, one for the Global registers and one for the DMA registers. See Table 2-5.

Table 2-5: Base Address Registers Definition for PCI Express

Register	Offset	Size	Function
Base Address 0	0010 (H)	8 MB	Node memory space
Base Address 2	0018 (H)	4 KB	Global registers
Base Address 4	0020 (H)	8 KB	DMA registers

Note: Each Base Address Register contains 32 bits. Since the PCI Express board uses 64-bit address space, each memory page covers two base addresses (0 – 1, 2 – 3, 4 – 5).

Tables 2-6 and 2-7 describe the bits of the Base Address Register.

Table 2-6: Base Address Register for PCI

Bit	Description
04 – 31	Address of memory region (with lower 4 bits removed)
03	Always 0 – memory is not prefetchable
01 – 02	Always 0 – memory may be mapped anywhere within the 32-bit memory space
00	Always 0 – indicates memory space

Table 2-7: Base Address Register for PCI Express

Bit	Description
04 – 31	Address of memory region (with lower 4 bits removed)
03	Always 1 – memory is prefetchable
01 – 02	Always 2 – memory may be mapped anywhere within the 64-bit memory space
00	Always 0 – indicates memory space

2.3.12 Cardbus CIS Pointer

Address: 0028 (H) Length: 32 bits

Read Only

This register is not implemented on the *EXC-1394PCI[e]*. The value at power-up is 0000 (H).

2.3.13 Subsystem ID

Address: 002C (H) Length: 16 bits

Read Only

The value at power-up is 0000 (H).

2.3.14 Subvendor ID

Address: 002E (H) Length: 16 bits

Read Only

The value at power-up is 0000 (H).

2.3.15 Expansion ROM Base Address Register (XROM)

Address: 0030 (H) Length: 32 bits

Read Only

This register is not implemented on the *EXC-1394PCI[e]*. The value at power-up is 0000 (H).

2.3.16 PCI Capabilities Pointer

Address: 0034 (H) Length: 8 bits

Read Only

The PCI Capabilities Pointer (Cap. Pointer) indicates the location of the PCI Capabilities Identification (ID) Register. The Capabilities ID Register stores a pointer to a structure within the configuration space. With a known Capabilities ID value, the associated structure can be found during the scanning process. The value at power-up is 0050 (H).

2.3.17 Interrupt Line Register (INTLN)

Address: 003C (H) Length: 8 bits

Read Only

This register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 0001 to 000F (H) correspond with the IRQ numbers 1 through 15, and the values from 0010 (H) to 00FE (H) are

reserved. The value of 255 signifies either “unknown” or “no connection” for the system interrupt. The value at power-up is 0000 (H).

2.3.18 Interrupt Pin Register (INTPIN)

Address: 003D (H) Length: 8 bits

Read Only

The value of this register is set to INTA#. The value at power-up is 0001 (H).

2.3.19 Minimum Grant Register (MINGNT)

Address: 003E (H) Length: 8 bits

Read Only

This register is not implemented on the *EXC-1394PCI[e]*. The value at power-up is 0000 (H).

2.3.20 Maximum Latency Register (MAXLAT)

Address: 003F (H) Length: 8 bits

Read Only

This register is not implemented on the *EXC-1394PCI[e]*. The value at power-up is 0000 (H).

2.4 DMA Registers (for PCI Express)

Direct Memory Access (DMA) enables the *EXC-1394PCIe* board to access system memory for reading and writing independently of the computer’s CPU. This results in faster data transfer to and from the board, with much less CPU overhead than when not using DMA.

There are two DMA channels:

- **DMA0** – DMA channel 0 is used for DMA writes
- **DMA1** – DMA channel 1 is used for DMA reads

Reserved		0044 – 1FFF (H)
Base Address for DMA0 and DMA1 Transfers		0040 (H)
Reserved		0038 (H)
Reserved (Bits 2 – 31)	DMA Interrupt Status (Bits 0 – 1)	0034 (H)
Reserved		0030 (H)
Reserved		0028 (H)
Reserved		0024 (H)
Reserved		0020 (H)
DMA1 Control		001C (H)
DMA1 Data Transfer Size		0018 (H)
DMA1 Address of Contiguous Host Memory – High 32 bits		0014 (H)
DMA1 Address of Contiguous Host Memory – Low 32 bits		0010 (H)
DMA0 Control		000C (H)
DMA0 Data Transfer Size		0008 (H)
DMA0 Address of Contiguous Host Memory – High 32 bits		0004 (H)
DMA0 Address of Contiguous Host Memory – Low 32 bits		0000 (H)

Figure 2-3: DMA Registers Map

2.4.1 DMA0 Address of Contiguous Host Memory

Address: 0000 (H) Length: 32 bits (Low)
Address: 0004 (H) Length: 32 bits (High)

Read/Write

The start address of the Contiguous Host Memory must be written to this register by the user. The address stored in this register is automatically incremented during the process of the DMA transfer. The current value in this register is the address following (the address of) the last requested data. Upon successful completion of a transfer, this register contains the following value: Start Address + Write Transfer Size, where Start Address is the start address of the Contiguous Host Memory.

2.4.2 DMA0 Data Transfer Size

Address: 0008(H) Length: 32 bits

Read/Write

This register contains the total amount of data (in bytes) to be written during a DMA write transfer. The total transfer size must be written to this register by the user. The transfer size value stored in this register is automatically decremented during the process of the DMA transfer. The current value stored indicates the remaining amount of data that needs to be transferred. Upon successful completion of a DMA write transfer, the value of this register should be 0.

2.4.3 DMA0 Control Register

Address: 000C (H) Length: 32 bits

Read/Write

This register contains information about, and controls, the DMA write data transfer.

Table 2-8: DMA0 Control Register

Bit	Description	
12 – 31	Reserved – set to 0	
08 – 11	DMA channel state	These bits describe the state of the DMA write channel. 0000 = (idle state) Last transfer ended successfully 0001 = (idle state) Last transfer was stopped by a node 0010 = (idle state) Last transfer ended because of CPL timeout 0011 = (idle state) Last transfer ended because of CPL UR error 0100 = (idle state) Last transfer ended because of CPL CA error 0101 – 0111 = (idle state) Reserved 1000 = (busy state) DMA channel is busy processing 1001 = (busy state) Requesting transfer. The DMA channel is in the process of requesting data from the host computer 1010 = (busy state) The DMA channel is waiting for completion of a read data transfer in response to a DMA read request 1011 = (busy state) Waiting for board to provide/accept data. The DMA channel is waiting for completion of a data transfer to or from the internal node memory. 1100 – 1111 = (busy state) Reserved
04 – 07	Reserved – set to 0	
03	Abort DMA transfer	1 = Abort transfer 0 = no effect
02	Start DMA transfer	1 = Start DMA transfer 0 = no effect
00 – 01	Reserved – set to 0	

2.4.4 DMA1 Address of Contiguous Host Memory

Address: 0010 (H) Length: 32 bits (Low)

Address: 0014 (H) Length: 32 bits (High)

Read/Write

The start address of the Contiguous Host Memory must be written to this register by the user. The address stored in this register is automatically incremented during the process of the DMA transfer. The current value in this register is the address following (the address of) the last requested data. Upon successful completion of a transfer, this register contains the following value: Start Address + Read Transfer Size, where Start Address is the start address of the Contiguous Host Memory.

2.4.5 DMA1 Data Transfer Size

Address: 0018 (H) Length: 32 bits

Read/Write

This register contains the total amount of data (in bytes) to be read during a DMA read transfer. The total transfer size must be written to this register by the user. The transfer size value stored in this register is automatically decremented during the process of the DMA transfer. The current value stored indicates the remaining amount of data that needs to be transferred. Upon successful completion of a DMA read transfer, the value of this register should be 0.

2.4.6 DMA1 Control Register

Address: 001C (H) Length: 32 bits

Read/Write

This register contains information about, and controls, the DMA read data transfer.

Table 2-9: DMA1 Control Register

Bit	Description	
12 – 31	Reserved – set to 0	
08 – 11	DMA channel state	These bits describe the state of the DMA read channel. 0000 = (idle state) Last transfer ended successfully 0001 = (idle state) Last transfer was stopped by a node 0010 = (idle state) Last transfer ended because of CPL timeout 0011 = (idle state) Last transfer ended because of CPL UR error 0100 = (idle state) Last transfer ended because of CPL CA error 0101 – 0111 = (idle state) Reserved 1000 = (busy state) DMA channel is busy processing 1001 = (busy state) Requesting transfer. The DMA channel is in the process of requesting data from the host computer 1010 = (busy state) The DMA channel is waiting for completion of a read data transfer in response to a DMA read request 1011 = (busy state) Waiting for board to provide/accept data. The DMA channel is waiting for completion of a data transfer to or from the internal node memory. 1100 – 1111 = (busy state) Reserved
04 – 07	Reserved – set to 0	
03	Abort DMA transfer	1 = Abort transfer 0 = no effect
02	Start DMA transfer	1 = Start DMA transfer 0 = no effect
00 – 01	Reserved – set to 0	

2.4.7 DMA Interrupt Status Register

Address: 0034 (H) Length: 2 bits

Read/Write (Write '1' to Clear)

Bit 0 of this register is set upon completion of a DMA transfer on DMA0, a DMA write. Bit 1 is set upon completion of a DMA transfer on DMA1, a DMA read. To clear either bit, write a 1 to the corresponding location.

Note: The two bits of the DMA Interrupt Status Register work together with the four bits of the Global Interrupt Status Register. When any of these six bits are set, an interrupt is generated. To locate the source of an interrupt, both of these registers need to be read.

In order to reset the interrupt, you must reset the appropriate bits of **both** the DMA Interrupt Status Register **and** the Global Interrupt Reset Register. See Interrupt Status Register on page 2-16.

2.4.8 Base Address for DMA0 and DMA1 Transfers

Address: 0040 (H) Length: 32 bits

Read/Write

This register contains the start address of the current DMA transfer (read or write transfer). The base must be written to this register by the user.

2.5 Node Memory Space Map

The node memory space map resides in the first memory block. Each node is allocated a space of 2 MB. See Figure 2-4 for the memory space mapping.

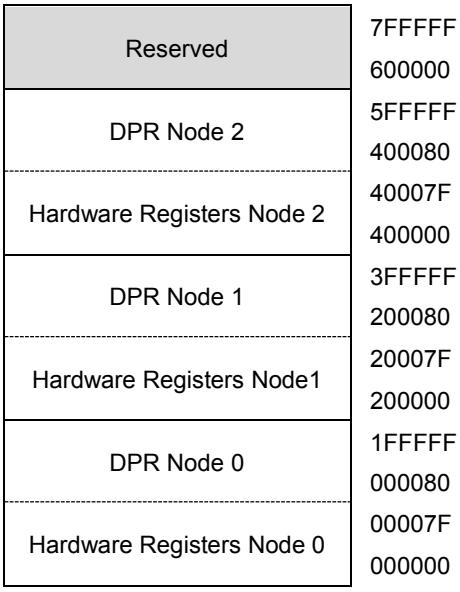

Figure 2-4: Node Memory Space Map

2.6 Global Registers Map

The board global registers reside in the second memory block.

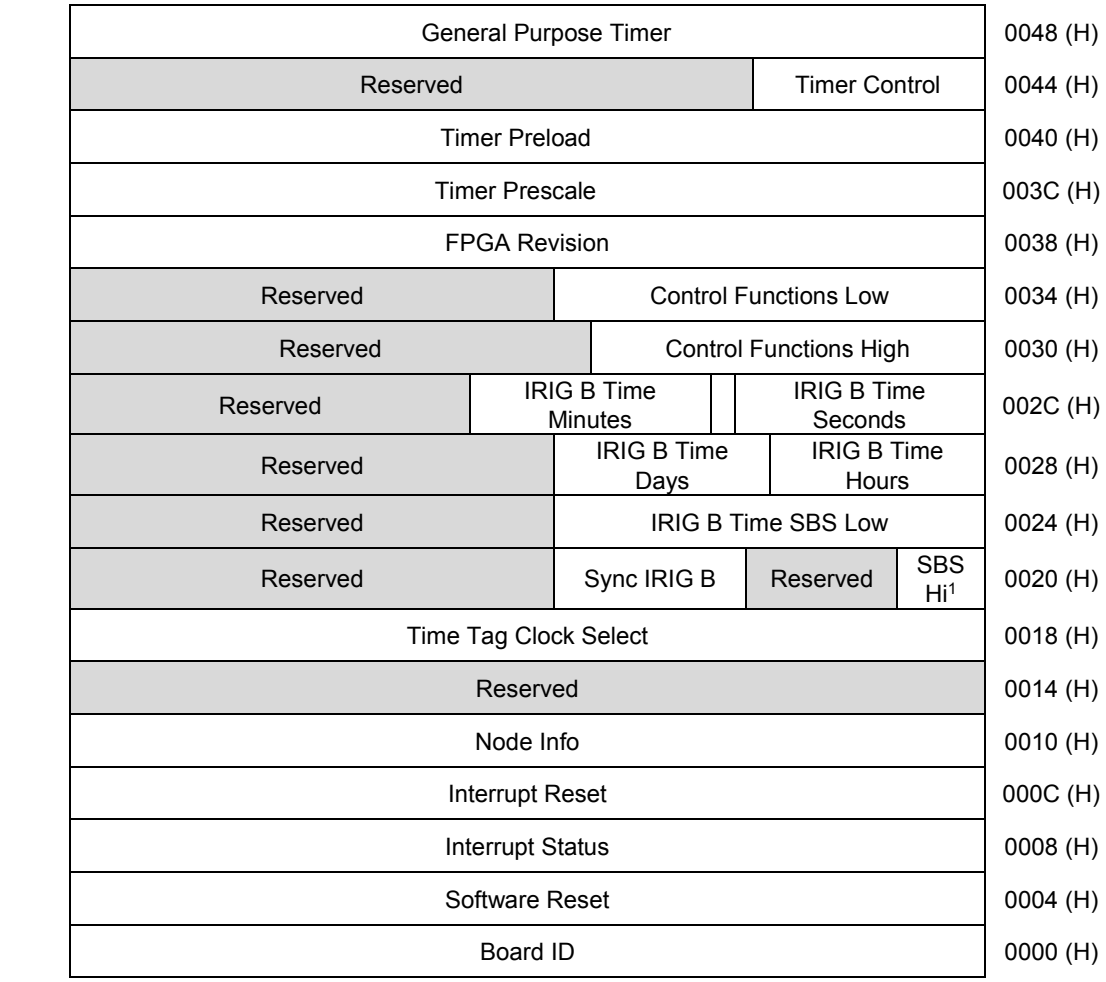

Figure 2-5: *EXC-1394PCI[e]* Global and IRIG B Registers Map

[1] IRIG B Time SBS Hi Register

2.6.1 Board Identification Register

Address: 0000 (H) Length: 32 bits

Read Only

Table 2-10: Board Identification Register

Bit	Description
16 – 31	Hard coded to the value 1394 (H)
12 – 15	**For PCI:** Hard coded to the value of 0 (H) **For PCI Express:** Hard coded to the value of E (H)
04 – 11	Reserved – set to 0
00 – 03	DIP switch selected ID

2.6.2 Software Reset Register

Address: 0004 (H) Length: 32 bits

Write Only

Use this register to perform reset operations of the nodes. Individual nodes can be reset.

Bit 04, the Global Time Tag reset bit, resets all the node Time Tag counters.

Table 2-11: Software Reset Register

Bit	Description	
05 – 31	Reserved – set to 0	
04	Global Time Tag reset	1 = reset all Time Tag counters 0 = no effect
03	Reserved – set to 0	
02	Node 2 reset	1 = reset node 0 = no effect
01	Node 1 reset	1 = reset node 0 = no effect
00	Node 0 reset	1 = reset node 0 = no effect

2.6.3 Interrupt Status Register

Address: 0008 (H) Length: 32 bits

Read Only

This register indicates which nodes are currently interrupting or if the General Purpose Timer has produced an interrupt.

Table 2-12: Interrupt Status Register

Bit	Description
04 – 31	Reserved – set to 0
03	1 = indicates that an interrupt was generated by the General Purpose Timer (See Global Timer Registers on page 2-22)
02	1 = indicates that node 2 is interrupting
01	1 = indicates that node 1 is interrupting
00	1 = indicates that node 0 is interrupting

Note: When using DMA, this register works together with the DMA Interrupt Status Register. See DMA Interrupt Status Register on page 2-14.

2.6.4 Interrupt Reset Register

Address: 000C (H) Length: 32 bits

Write Only

Use this register to reset the interrupting nodes by writing to the relevant bits of the register.

Table 2-13: Interrupt Reset Register

Bit	Description
04 – 31	Reserved – set to 0
03	1 = Resets General Purpose Timer interrupt 0 = No effect
02	1 = Resets node 2 interrupt 0 = No effect
01	1 = Resets node 1 interrupt 0 = No effect
00	1 = Resets node 0 interrupt 0 = No effect

Note: When using DMA, this register works together with the DMA Interrupt Status Register. See DMA Interrupt Status Register on page 2-14.

2.6.5 Node Info Registers

Address: 0010 (H) Length: 32 bits

Read Only

These registers provide information for each of the 3 channel, respectively.

Table 2-14: Node Info Registers

Bit	Description	
00 – 02	Node ID	0000 (H) = Node 0 Info Register 0001 (H) = Node 1 Info Register 0002 (H) = Node 2 Info Register
05 – 31	Reserved – set to 0	

2.6.6 Time Tag Clock Select Register

Address: 0018 (H) Length: 32 bits

Read/Write

Use this register to set either an internal (10 MHz) or external source for the board's Global Time Tag Clock. For details on the External Time Tag Clock, see Communications I/O Connector [J1] on page 8-4.

Table 2-15: Time Tag Clock Select Register

Bit	Description	
01 – 31	Reserved – set to 0	
00	Time Tag Clock Select	1 = External Source 0 = Internal Source (Default)

2.7 IRIG B Global Registers

The *EXC-1394PCI[e]* is able to receive and decode standard serial IRIG B120 time code format signals via its External Signal Connector J1. See Communications I/O Connector [J1] on page 8-4.

IRIG B120 signals have the following specifications:

B = 100 pulses per second (PPS), 10 msec count

1 = Sine wave carrier, amplitude modulated

2 = 1 kHz carrier wave (1 msec resolution)

0 = Binary Coded Decimal (BCD), Control Functions (CF) depending on the user application, Straight Binary Second (SBS) of day (0 – 86400)

For more information, visit irig.org.

The IRIG B signal, which contains 3 types of words within each Time Code Frame, can be used to synchronize the Time Tags of the nodes on the *EXC-1394PCI[e]*.

1st Word	Time-of-year in binary coded decimal (BCD) notation in hours, minutes and seconds.
2nd Word	Set of bits reserved for decoding various control, identification and other special purpose functions.
3rd Word	Seconds-of-day weighted in straight binary seconds (SBS) notation

These three words can be stored and displayed in the IRIG B global registers 0020 – 002B (H).

For the location of the registers on the memory map, see *Global* Registers Map on page 2-15.

Note: The synchronization of IRIG B time can take up to two seconds. IRIG B functions are meant to be used on an occasional basis, not on a constant basis.

2.7.1 Sync IRIG B Register

Address: 0020 (H) Bits 08 – 10

Read/Write

Use this register to control the synchronization of a node's Time Tags relative to the IRIG B input signal and the display of the IRIG B time within the IRIG B Time registers.

Table 2-16: Sync IRIG B Register

Bit	Description
10	1 = Set by board to indicate that the current IRIG B time has been stored in the IRIG B registers 0 = No IRIG B time has been stored in the IRIG B registers. This bit must be reset after the board has written a '1'.
09	1 = Stores and displays the IRIG B time and control functions into the 6 IRIG B registers (0014 – 001E (H)) corresponding to the previous valid IRIG B message. If bit 08 is set, then the IRIG B time is stored at the same time that the Time Tags are reset. To calculate the real time to which the Time Tags are synchronized, **add** '1' to the value of the IRIG B time stored into these registers. 0 = The previous valid IRIG B message should not be stored in the IRIG B registers. This bit is automatically reset by the board after the storage of the IRIG B time.
08	1 = Resets and synchronizes Time Tags of all the nodes to the next rising edge of the on-time Reference Point **Pr** of the IRIG B signal. Also sets Bit 09 to a value of '1' in order to store and display the IRIG B time and control functions into the 6 IRIG B registers. 0 = No reset/synchronization of Time Tags relative to the **Pr** of the IRIG B signal. This bit is automatically reset by board after reset of Time Tags.

Note: All bits are read and write.

2.7.2 IRIG B Time SBS High Register

Address: 0020 (H) Bit 0

Read Only

This register contains the MSB of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.7.3 IRIG B Time SBS Low Register

Address: 0024 (H) Bits 0 – 15

Read Only

This register contains the lower 16 bits of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.7.4 IRIG B Time Days Register

Address: 0028 (H) Bits 6 – 15

Read Only

This register contains the days value of the BCD time-of-year subword within the IRIG B coded message.

2.7.5 IRIG B Time Hours Register

Address: 0028 (H) Bits 0 – 5

Read Only

This register contains the hours value of the BCD time-of-year subword within the IRIG B coded message.

2.7.6 IRIG B Time Minutes Register

Address: 002C (H) Bits 8 – 14

Read Only

This register contains the minutes value of the BCD time-of-year subword within the IRIG B coded message.

2.7.7 IRIG B Time Seconds Register

Address: 002C (H) Bits 0 – 6

Read Only

This register contains the seconds value of the BCD time-of-year subword within the IRIG B coded message.

2.7.8 Control Functions High and Low Registers

Address: 0030 (H) Bits 0 – 10 (High)

Address: 0034 (H) Bits 0 – 15 (Low)

Read Only

The IRIG B time code formats reserve 27 bits known as Control Functions. The Control Functions are for user-defined encoding of various control, identification or other special purpose functions. No standard coding system exists. The control bits may be programmed in any predetermined coding system.

2.7.9 FPGA Revision Register

Address: 0038 (H) Bits 0– 31

Read Only

This register contains the FPGA revision of the board.

2.8 Global Timer Registers

For the location of the registers on the memory map, see *Global* Registers Map on page 2-15.

2.8.1 Timer Prescale Register

Address: 003C (H) Bits 0 – 31

Read/Write

Use this register to define the resolution of the General Purpose Timer. It is based on the Global Time Tag Clock (nominally 1 MHz) and provides the General Purpose Timer resolution as follows:

Table 2-17: Timer Prescale/General Purpose Timer Resolution

Timer Prescale Register Value (DEC)	General Purpose Time Resolution (μsec)
0 or 1	1 (default)
2	2
3	3
•	•
•	•
•	•
10	10
•	•
•	•
•	•
65535	65535

Note: The Timer Prescale Register can only be changed when the timer has been stopped.

2.8.2 Timer Preload Register

Address: 0040 (H) Bits 0 – 31

Read/Write

Use this register to set the starting count value for the General Purpose Timer from which it will start to count down. The Timer Preload Register can only be changed while the timer is stopped and has a maximum count value of 65535.

Note: The General Purpose Timer will not start counting if a value of zero is stored in the Timer Preload Register.

Default value: 00 00

2.8.3 Timer Control Register

Address: 0044 (H) Bits 0 – 3

Read/Write

Use this register to control the General Purpose Timer Register. The value stored in bits 01 to 03 take effect when the General Purpose timer reaches a value of zero. Bit 0 is used to start and stop the General Purpose Timer. The values of bits 01 – 03 can only be changed when the General Purpose Timer Register is stopped.

Default value: 00 00

Table 2-18: Timer Control Register

Bit	Description	
04 – 15	Reserved – set to 0	
03	Global reset on count completed	1 = Causes global reset of all installed nodes 0 = No effect
02	Interrupt on count completed	1 = Output an interrupt (see Interrupt Status Register on page 2-16) 0 = No effect
01	Reload mode	1 = Reload mode 0 = Non-reload/One-shot mode
00	Start/Stop	1 = Start 0 = Stop

2.8.4 General Purpose Timer Register

Address: 0048 (H) Bits 0 – 31

Read Only

This register stores the current count value of the General Purpose Timer. The General Purpose Timer is controlled by the Timer Control Register. When the General Purpose Timer is started it counts down to zero, at which point either an interrupt can be generated and or all installed nodes can be reset.

If the General Purpose Timer is in reload mode then the current value in Timer Preload Register is stored into the General Purpose Timer and the timer starts to count down from this value.

If the General Purpose Timer is in non-reload/one shot mode, when it reaches zero it stops, and a value of zero is displayed in the General Purpose Timer Register. In this case, Bit 0 (the Start/Stop bit) of the Timer Control Register is automatically set to zero. If the General purpose Timer Register is then started, it starts to count from the current Timer Preload Register value automatically (without the need to do a write to the Timer Preload Register).

At any point in time, the General Purpose Timer can be stopped at the current count value. When a start is then issued, the General purpose Timer starts to count down from this current count value. If you want to stop the counter and start from the original preload value or from a new preload value, this value must to be rewritten

to the Timer Preload Register prior to the restarting of the General Purpose Timer Register.

Note: The maximum clock period of the General Purpose Timer is 4295 seconds (1 hour, 11 min & 35 Seconds).

Chapter 3 Node Operation Overview

Chapter 3 provides a general overview of the operation of each of the *EXC-1394PCI[e]* nodes.

3.1 Node General Memory Map

Each node occupies 2 MB of memory space that is shared between the hardware registers, control registers and data blocks.

Each node can operate in one of the following modes:

- CC mode
- RN mode
- Bus Monitor mode
- Asyncronous mode

For a description of each mode, see Overview on page 1-1.

Table 3-1 indicates which areas of memory are mode-specific, and which areas are common to all modes. Memory maps for each specific mode are provided in the chapters 4 through 7, as well as description of the registers in each mode.

Table 3-1: Node General Memory Map

Register Name	Byte Address
Hardware Revision Register	0000 (H)
Excalibur Node ID Register	0002 (H)
Interrupt Status Register	0004 (H)
Interrupt Mask Register	0008 (H)
Reset Time Register	000C (H)
Reserved	000E – 000F (H)
Time Tag Low Register	0010 (H)
Time Tag Middle Register	0012 (H)
Time Tag High Register	0014 (H)
Reserved	0016 – 0017 (H)
Mode Specific Registers	0018 – 0019 (H)
Reserved	001A – 001B (H)
Mode Specific Registers	001C – 001F (H)
Reserved	0020 – 007F (H)
Mode Specific Registers	0080 (H)
Reserved	0084 – 0087 (H)
Receive Message Counter Register	0088 (H)
Reserved	008C – 008F (H)
STOF Message Counter Register (reserved in Asynchronous mode)	0090 (H)

Register Name	Byte Address
Reserved	0094 – 0097 (H)
Receive Message Error Counter Register	0098 (H)
Reserved	009C – 009F (H)
Discarded Message Counter Register	00A0 (H)
Reserved	00A4 – 00A7 (H)
Firmware Revision Register	00A8 (H)
Mode Specific Registers	00AC (H)
Mode Select Register	00B0 (H)
Start Register	00B4 (H)
Excalibur Node Status Register	00B8 (H)
Port Status Register	00BC (H)
Mode Specific Registers	00C0 – 00F1 (H)
Reserved	00F2 – 00F3 (H)
Options Register	00F4 – 00F7 (H)
Reserved	00F8 – 00FF (H)
STOF Period Register (reserved in Asynchronous mode)	0100 (H)
Last STOF Message Status Register (reserved in Asynchronous mode)	0102 (H)
Last STOF Message Area (reserved in Asynchronous mode)	0104 – 012F (H)
Last STOF Time Tag Registers (reserved in Asynchronous mode)	0130 (H)
Reserved	0136 – 0137 (H)
Mode Specific Registers	0138 – 138FF (H)
Message Area	13900 – 1FFFFF (H)

Chapter 4 Control Computer Operation

Chapter 4 describes operation in Control Computer (CC) mode. In CC mode, the node acts as the Root Node and Bus Manager, and is responsible for sending out the STOF message at a precise, predefined, programmable interval. It has two Transmit Stacks, one for Single-Shot and one for Continuous, to allow the first frame to be configured differently than the other frames. The node has programmable STOF offsets for each RN with two receive offsets for each RN: one for the Single-Shot Stack and one for the Continuous Stack. Receive messages can be filtered by a combination of message number and transmitting RN (message type). Interrupts can be requested for all messages or for specific message types, as well as for various error conditions.

There are three possible transmission modes:

- Continuous
- Single-Shot
- Both stacks – In this mode, the Single-Shot stack is transmitted once, and the Continuous stack is transmitted continuously thereafter. (This is useful in a scenario where the first frame must be according to the original preset offsets. The CC updates the RNs with new offsets, which are used in all subsequent frames).

The following topics are covered:

4.1 CC Memory Map 4-2

4.2 CC Mode Register Definitions 4-4

4.2.1 Hardware Revision Register 4-4
4.2.2 Excalibur Node ID Register 4-4
4.2.3 Interrupt Status Register 4-4
4.2.4 Interrupt Mask Register 4-5
4.2.5 Reset Time Register 4-6
4.2.6 Time Tag Registers 4-6
4.2.7 Reset Node Register 4-7
4.2.8 Vehicle Time Preload Value Register 4-7
4.2.9 Transmit Message Counter Register 4-7
4.2.10 Receive Message Counter Register 4-8
4.2.11 STOF Message Counter Register 4-8
4.2.12 Receive Message Error Counter Register 4-8
4.2.13 Transmit Message Error Counter Register 4-8
4.2.14 Discarded Message Counter Register 4-9
4.2.15 Firmware Revision Register 4-9
4.2.16 Pointer to Current Entry of Transmit Stack 4-9
4.2.17 Mode Select Register 4-9
4.2.18 Start Register 4-10
4.2.19 Excalibur Node Status Register 4-10
4.2.20 Port Status Register 4-11
4.2.21 1394 Node ID Register 4-13
4.2.22 CC Run Configuration Register 4-13
4.2.23 Pointer to Beginning of Single-Shot Stack 4-13
4.2.24 Pointer to Beginning of Continuous Mode Stack 4-14
4.2.25 Pointer to Beginning of Receive Linked List 4-14
4.2.26 Pointer to End of Receive Linked List 4-14
4.2.27 Speed Code Register 4-14
4.2.28 Options Register 4-15
4.2.29 STOF Period Register 4-15

4.2.30 Last STOF Message Status Register 4-15
4.2.31 Last STOF Message Area 4-16
4.2.32 Last STOF Time Tag Registers 4-16
4.2.33 Pointer to Most Recent Message 4-17
4.2.34 Pointer to Least Recent Message 4-17
4.2.35 Message Type Receive Control Table 4-17
4.2.36 CC STOF Offsets Table 4-18
4.3 Message Area 4-18
4.3.1 CC Transmit Messages 4-18
4.3.2 CC Transmit Stacks 4-19
4.3.3 CC Linked List Area 4-21

4.1 CC Memory Map

Table 4-1: CC Mode Memory Map Registers

Register Name	Byte Address	Read/Write	Page Number
Hardware Revision Register	0000 (H)	Read Only	4-4
Excalibur Node ID Register	0002 (H)	Read Only	4-4
Interrupt Status Register	0004 (H)	Read/Write (Write '1' to Clear)	4-4
Interrupt Mask Register	0008 (H)	Read/Write	4-5
Reset Time Register	000C (H)	Read/Write	4-6
Reserved	000E – 000F (H)		
Time Tag Low Register	0010 (H)	Read Only	4-6
Time Tag Middle Register	0012 (H)	Read Only	4-6
Time Tag High Register	0014 (H)	Read Only	4-6
Reserved	0016 – 0017H		
Reset Node Register	0018 (H)	Write Only	4-7
Reserved	001A – 001B (H)		
Vehicle Time Preload Value Register	001C	Read/Write	4-7
Reserved	0020 – 007F (H)		
Transmit Message Counter Register	0080 (H)	Read Only	4-7
Reserved	0084 – 0087 (H)		
Receive Message Counter Register	0088 (H)	Read Only	4-8
Reserved	008C – 008F (H)		
STOF Message Counter Register	0090 (H)	Read Only	4-8
Reserved	0094 – 0097 (H)		
Receive Message Error Counter Register	0098 (H)	Read Only	4-8
Transmit Message Error Counter Register	009C (H)	Read Only	4-8
Discarded Message Counter Register	00A0 (H)	Read Only	4-9
Reserved	00A4 – 00A7 (H)		

Register Name	Byte Address	Read/Write	Page Number
Firmware Revision Register	00A8 (H)	Read Only	4-9
Pointer to Current Entry of Transmit Stack	00AC (H)	Read Only	4-9
Mode Select Register	00B0 (H)	Read/Write	4-9
Start Register	00B4 (H)	Read/Write	4-10
Excalibur Node Status Register	00B8 (H)	Read Only	4-10
Port Status Register	00BC (H)	Read Only	4-11
Reserved	00C0 – 00C7 (H)		
1394 Node ID Register	00C8 (H)	Read Only	4-13
CC Run Configuration Register	00CC (H)	Read/Write	4-13
Pointer to Beginning of Single-Shot Stack	00D0 (H)	Read/Write	4-13
Pointer to Beginning of Continuous Mode Stack	00D4 (H)	Read/Write	4-14
Pointer to Beginning of Receive Linked List	00D8 (H)	Read/Write	4-14
Pointer to End of Receive Linked List	00DC (H)	Read/Write	4-14
Reserved	00E0 – 00EF (H)		
Speed Code Register	00F0 (H)	Read/Write	4-14
Reserved	00F2 – 00F3 (H)		
Options Register	00F4 – 00F7 (H)	Read Only	4-15
Reserved	00F8 – 00FF (H)		
STOF Period Register	0100 (H)	Read/Write	4-15
Last STOF Message Status Register	0102 (H)	Read/Write	4-15
Last STOF Message Area	0104 – 012F (H)	Read Only	4-16
Last STOF Time Tag Registers	0130 (H)	Read Only	4-16
Reserved	0136 – 013B		
Pointer to Most Recent Message	013C (H)	Read Only	4-17
Pointer to Least Recent Message	0140 (H)	Read Only	4-17
Reserved	0144 – 02FF (H)		
Message Type Receive Control Table	0300 – 34FF (H)	Read/Write	4-17
CC STOF Offsets Table	3500 – 38FF (H)	Read/Write	4-18
Message Area	3900 – 1FFFFF (H)	Read/Write	4-18

4.2 CC Mode Register Definitions

4.2.1 Hardware Revision Register

Address: 0000 (H) Length: 16 bits

Read Only

This register contains the revision number of the hardware logic. 12 bits are used for the major revision, and four bits are used for the minor revision. For example, for hardware revision 2.1, 2 is stored in the high 12 bits, and 1 is stored in the low four bits.

4.2.2 Excalibur Node ID Register

Address: 0002 (H) Length: 16 bits

Read Only

This register contains the identifier of the Excalibur Node. This is set to 1394 (H).

4.2.3 Interrupt Status Register

Address: 0004 (H) Length: 32 bits

Read/Write (Write '1' to Clear)

This register indicates the occurrence various interrupt events or conditions. Each bit indicates the occurrence of a specific event/condition. The bits in this register are lit when the event/condition occurs, regardless of whether the event/condition is set to generate an interrupt. For information on generating interrupts, see the Interrupt Mask Register on page 4-5.

Table 4-2: Interrupt Status Register

Bit	Description
31	Interrupt occurred on end of message (transmit) for a specific message (queuing complete; can change the data). Check Stack Status Words for which message.
30	Interrupt occurred on start of message (transmit) for a specific message (queuing in progress; can change the data pointer). Check Stack Status Words for which message.
29	Interrupt occurred on end of message (receive) for a specific message. Check Linked List Status Words for which message.
15 – 28	Reserved
14	End of buffer reached
13	Buffer midpoint reached
07 – 12	Reserved
06	STOF transmit complete
05	End of message queuing (transmit)
04	Start of message (transmit)
03	End of message (receive)
02	Reserved
01	Reserved
00	Message error

4.2.4 Interrupt Mask Register

Address: 0008 (H) Length: 32 bits

Read/Write

Use this register to set interrupts. Each bit is a flag that enables or disables the generation of a specific interrupt.

When an interrupt is received, check the Interrupt Status Register to see which condition (or conditions) caused the interrupt.

Table 4-3: Interrupt Mask Register

Bit	Description
15 – 31	Reserved
14	Interrupt on end of buffer reached
13	Interrupt on buffer midpoint reached
07 – 12	Reserved
06	Interrupt on end of STOF transmit
05	Interrupt on end of Transmit Stack message
04	Interrupt on start of Transmit Stack message
03	Interrupt on end of received message
02	Reserved
01	Reserved
00	Interrupt on message error

4.2.5 Reset Time Register

Address: 000C (H) Length: 16 bits

Read/Write

Use this register to reset the node's Time Tag and vehicle time.

Table 4-4: Reset Time Register

Bit	Description
02 – 15	Reserved
01	Reset vehicle time (Resets the vehicle time to the value set in the Vehicle Time Preload Value Register. See page 4-7. This is the timer used to fill in the Vehicle time field in the STOF messages.)
00	Reset Time Tag (Resets the Time Tag to 0. All message Time Tags, STOF offsets and STOF timing are based on this Time Tag value)

4.2.6 Time Tag Registers

Address: 0010 (H) Length: 48 bits

Read Only

These three registers represent the current value of the Time Tag. All message Time Tags, STOF offsets and STOF timing are based on this Time Tag value. The Time Tag has a precision of 100 nanoseconds per bit. The Time Tag should be read from address 10 then 12 then 14. When reading address 10 the Time Tag registers are frozen, reading address 14 unfreezes them.

Table 4-5: Time Tag Registers

Address	Description
10	Low 16 bits of Time Tag
12	Middle 16 bits of Time Tag
14	High 16 bits of Time Tag

4.2.7 Reset Node Register

Address: 0018 (H) Length: 16 bits

Write Only

Use this register to reset the node.

Table 4-6: Reset Node Register

Bit	Description
01 – 15	Reserved
00	Reset Node (resets the node, clears the control registers and resets the Time Tag)

4.2.8 Vehicle Time Preload Value Register

Address: 001C (H) Length: 32 bits

Read/Write

Use this register to set the initial (default) value of the vehicle time timer, that will be used when the timer is reset. The vehicle time is in units of 25 μsec.

Table 4-7: Vehicle Time Preload Value

Bit	Description
00 – 32	Vehicle time

4.2.9 Transmit Message Counter Register

Address: 0080 (H) Length: 32 bits

Read Only

This register contains a running count of all messages transmitted by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 4-8: Transmit Message Counter Register

Bit	Description
00 – 31	Number of messages transmitted by the node

4.2.10 Receive Message Counter Register

Address: 0088 (H) Length: 32 bits

Read Only

This register contains a running count of all messages received and stored by the node. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 4-9: Receive Message Counter Register

Bit	Description
00 – 31	Number of messages received and stored by the node

4.2.11 STOF Message Counter Register

Address: 0090 (H) Length: 32 bits

Read Only

This register contains a running count of all STOF messages transmitted by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 4-10: STOF Message Counter Register

Bit	Description
00 – 31	Number of STOF messages transmitted by the node

4.2.12 Receive Message Error Counter Register

Address: 0098 (H) Length: 32 bits

Read Only

This register contains a running count of all messages with errors received and stored. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 4-11: Receive Message Error Counter Register

Bit	Description
00 – 31	Number of messages with errors received and stored by the node

4.2.13 Transmit Message Error Counter Register

Address: 009C (H) Length: 32 bits

Read Only

This register contains a running count of all transmit messages with errors. It is reset to 0 upon power-up, node reset and when the node is started.

Table 4-12: Transmit Message Error Counter Register

Bit	Description
00 – 31	Number of transmit messages with errors

4.2.14 Discarded Message Counter Register

Address: 00A0 (H) Length: 32 bits

Read Only

This register contains a running count of all messages that were discarded by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 4-13: Discarded Message Counter Register

Bit	Description
00 – 31	Number of messages received and discarded by the node

4.2.15 Firmware Revision Register

Address: 00A8 (H) Length: 32 bits

Read Only

This register contains the revision number of the firmware running on the node. 16 bits are used for the major revision, and 16 bits are used for the minor revision. For example, for firmware revision 2.1, 2 is stored in the high 16 bits, and 1 is stored in the low 16 bits.

4.2.16 Pointer to Current Entry of Transmit Stack

Address: 00AC (H) Length: 32 bits

Read Only

This register contains a pointer to the location in the Transmit Stack that is currently being transmitted.

4.2.17 Mode Select Register

Address: 00B0 (H) Length: 32 bits

Read/Write

Use this register to select the operational mode of the node.

Table 4-14: Mode Select Register

Bit	Value	Description
00 – 31	0	Node was initialized, but was not yet set into an operational mode
	1	Remote Node (RN) Mode
	2	Control Computer (CC) Mode
	3	Bus Monitor Mode
	4	Asynchronous Mode

4.2.18 Start Register

Address: 00B4 (H) Length: 32 bits

Read/Write

Use this register to start and stop the operations of the node.

Table 4-15: Start Register

Bit	Description
01 – 31	Reserved
00	1 = Start Operation 0 = Stop Operation

4.2.19 Excalibur Node Status Register

Address: 00B8 (H) Length: 32 bits

Read Only

This register indicates the current status of the node. It also provides power-on self-test information.

Table 4-16: Excalibur Node Status Register

Bit	Description
31	Reserved
30	Message fragment detected (the receive FIFO had part of a message. There was probably an overrun or other technical glitch in receiving)
29	Out-of-frame message received (received a message before first STOF or after missing STOFs)
17 – 28	Reserved
16	Wrong LLC version (indicates that the link-layer chip had technical difficulties)
05 – 15	Reserved
04	1 = Running 0 = Halted
03	1 = Self Test Passed 0 = Self Test Failed
02	Reserved
01	1 = RAM test passed 0 = RAM test failed
00	1 = Ready 0 = Not ready

4.2.20 Port Status Register

Address: 00BC (H) Length: 32 bits

Read Only

This register indicates the status of the three ports.

Table 4-17: Port Status Register

Bit	Description
24 – 31	Reserved
23	Port 0 Connected
22	Port 0 Receive OK
21	Port 0 Beta Mode
20	Port 0 Bit 0 of maximum possible speed
19	Port 0 Bit 1 of maximum possible speed
18	Port 0 Bit 2 of maximum possible speed
17	Port 0 Spare
16	Port 0 Spare
15	Port 1 Connected
14	Port 1 Receive OK
13	Port 1 Beta Mode
12	Port 1 Bit 0 of maximum possible speed
11	Port 1 Bit 1 of maximum possible speed
10	Port 1 Bit 2 of maximum possible speed
09	Port 1 Spare
08	Port 1 Spare
07	Port 2 Connected
06	Port 2 Receive OK
05	Port 2 Beta Mode
04	Port 2 Bit 0 of maximum possible speed
03	Port 2 Bit 1 of maximum possible speed
02	Port 2 Bit 2 of maximum possible speed
01	Port 2 Spare
00	Port 2 Spare

Table 4-18: Port Speed Bits

Speed	Bit 2	Bit 1	Bit 0
100 Mbps	0	0	0
200 Mbps	0	0	1
400 Mbps	0	1	0
Not Supported	0	1	1
Not Supported	1	0	0

4.2.21 1394 Node ID Register

Address: 00C8 (H) Length: 32 bits

Read Only

This register contains the node ID assigned automatically during bus configuration.

Table 4-19: 1394 Node ID

Bit	Description
00 – 31	1394 Node ID

4.2.22 CC Run Configuration Register

Address: 00CC (H) Length: 32 bits

Read/Write

Use this register to specify the type of node operation, Single-Shot, Continuous, or a combination of the two: Single-Shot with transmission from the Single-Shot Stack, automatically followed by continuous transmission from the Continuous Stack. To select the combined option, set both bits to 1.

Table 4-20: CC Run Configuration Register

Bit	Description
03 – 31	Reserved
02	1 = Do not update the Vehicle Time quadlet of the STOF message before each STOF message is transmitted. (Any data provided by the user will be transmitted instead.) 0 = Allow the firmware to update the Vehicle Time quadlet of the STOF message before each STOF message is transmitted (default)
01	1 = Run for one STOF frame, transmitting from the Single-Shot Stack 0 = Do not run using the Single-Shot Stack (default)
00	1 = Run continuously, using Continuous Stack (default) 0 = Do not run continuously

4.2.23 Pointer to Beginning of Single-Shot Stack

Address: 00D0 (H) Length: 32 bits

Read/Write

Use this register to specify the address at which to put the beginning of the Single-Shot Transmit Message Stack.

4.2.24 Pointer to Beginning of Continuous Mode Stack

Address: 00D4 (H) Length: 32 bits

Read/Write

Use this register to specify the address at which to put the beginning of the Continuous Mode Transmit Message Stack.

4.2.25 Pointer to Beginning of Receive Linked List

Address: 00D8 (H) Length: 32 bits

Read/Write

Use this register to specify the address of the beginning of the received Linked List.

4.2.26 Pointer to End of Receive Linked List

Address: 00DC (H) Length: 32 bits

Read/Write

Use this register to specify the address of the end of the received Linked List.

4.2.27 Speed Code Register

Address: 00F0 (H) Length: 16 bits

Read/Write

Use this register to select the communications speed of the node.

Table 4-21: Speed Code Register

Bit	Description
02 – 15	Reserved
00 – 01	Speed Code

Table 4-22: Speed Code Bits

Speed	Bit 1	Speed Bit 0
100 Mbps	0	0
200 Mbps	0	1
400 Mbps	1	0
Not Supported	1	1

4.2.28 Options Register

Address: 00F4 (H) Length: 32 bits

Read Only

This register contains information about the node.

Table 4-23: Options Register

Bit	Description
02 – 15	Reserved
01	1 = By default, the Vehicle Time quadlet of each STOF message is updated before transmission (in CC mode). When this bit is lit, the option to prevent updating the Vehicle Time quadlet is available; see CC Run Configuration Register on page 4-13 0 = The option to prevent updating the Vehicle Time quadlet of the STOF message before transmission is not available
00	1 = Asynchronous mode is available 0 = Asynchronous mode is not available

4.2.29 STOF Period Register

Address: 0100 (H) Length: 16 bits

Read/Write

Use this register to set the period of time (in µsec) within which the STOF is expected to be received. The value of this register defaults to 12500 upon power-up and reset.

Table 4-24: STOF Period Register

Bit	Description
00 – 15	Period in µsec to transmit STOF

4.2.30 Last STOF Message Status Register

Address: 0102 (H) Length: 16 bits

Read/Write

This register contains the status of the STOF message area. Check this register to see whether the data in the STOF Message area and STOF Time Tag area are consistent and to check for errors in the STOF messages.

Table 4-25: Last STOF Message Status Register

Bit	Description
15	1 = STOF Complete – the parts of the STOF message data written by the node, and the Time Tag can be read 0 = STOF not available (e.g. no STOF has yet been sent) or in mid-update
14	STOF message queuing in progress (do not change or read the data or read the Time Tag)
01 – 13	Reserved
00	1 = error in STOF transmit 0 = no error

4.2.31 Last STOF Message Area

Address: 0104 (H) Length: 11 32-bit words

Read Only

This register contains information on the last STOF message transmitted by the node. It also contains the data for the next STOF message to be transmitted.

Table 4-26: Last STOF Message Area

Quadlet	Description	Read/Write
00	1394 Header Word	Read/Write
01	Control Computer Branch Status	Read/Write
02	Network Bus Mode	Read/Write
03	Vehicle State	Read/Write
04	Vehicle Time	Read Only
05 – 09	Reserved	N/A
10	Vertical Parity Check	Read Only

4.2.32 Last STOF Time Tag Registers

Address: 0130 (H) Length: 48 bits

Read Only

These three 16-bit registers represent the value of the node's Time Tag at the time the last STOF was transmitted.

Table 4-27: Last STOF Time Tag Registers

Word	Description
0	Low 16 bits of Time Tag
1	Middle 16 bits of Time Tag
2	High 16 bits of Time Tag

4.2.33 Pointer to Most Recent Message

Address: 013C (H) Length: 32 bits

Read Only

This register contains a pointer to the beginning of the last complete message received by the node.

Table 4-28: Pointer to Most Recent Message

Bit	Description
00 – 31	Pointer to sentinel of most recent message in the buffer

4.2.34 Pointer to Least Recent Message

Address: 0140 (H) Length: 32 bits

Read Only

This register contains a pointer to the beginning of the oldest complete message received by the node.

Table 4-29: Pointer to Least Recent Message

Bit	Description
00 – 31	Pointer to sentinel of the oldest message in the buffer

4.2.35 Message Type Receive Control Table

Between transmissions, the CC looks for receive messages. These messages are stored in a sequential Linked List. A data structure of 6400 by 16 bits contains a CC Receive Control Word for each potential message within each channel. This structure is a two dimensional array of 16 bit words indexed by source channel number and message number.

Note that the interrupt on end of message which can be set here is reflected in the Interrupt Status Register, bit 29.

Table 4-30 describes the fields of the CC Receive Control Word.

Table 4-30: CC Receive Control Word

Bit	Description
04 – 15	Reserved
03	Store/Do not Store
02	Reserved
01	Interrupt on end of message
00	Reserved

4.2.36 CC STOF Offsets Table

For each channel number, this table contains STOF offset information (in μsec). The table is indexed by channel number. The information must be filled in for each channel to which the CC will transmit messages. It is used to determine when to send out the message (at the appropriate receive offset). It is also used for generating the message trailer.

This table is read once, when CC mode is started. Changes made while running only take effect when the CC is stopped and restarted.

Table 4-31 describes the fields of each entry in the CC STOF Offsets Table.

Table 4-31: CC STOF Offsets Table

Word	Description
0 – 1	Initial receive offset (used for transmitting messages in the Single-Shot Stack)
2 – 3	Transmit Offset
4 – 5	Receive Offset (used for transmitting messages in the Continuous Stack)
6 – 7	Datapump offset

4.3 Message Area

The CC Message Area contains:

- CC Transmit Messages
- CC Transmit Stacks
- CC Linked List Area

4.3.1 CC Transmit Messages

Table 4-32 describes the fields of the Transmit Message Data Area.

Table 4-32: Transmit Message Data Area

Word	Description
0 – 1	1394 Header quadlet
2 – 9	ASM Header
Length based on payload length	Payload

Note: The data area must not contain the header CRC, the data CRC or the trailer. The trailer is comprised of the three STOF offsets and the VPC, and is automatically generated by the firmware based on the values in the STOF Offsets Table.

The interrupts which can be set in the Control Word are reflected in the Interrupt Status Register, bits 30 and 31. See Interrupt Mask Register on page 4-5.

Figure 4-1 shows the information that you must supply in a Transmit Message.

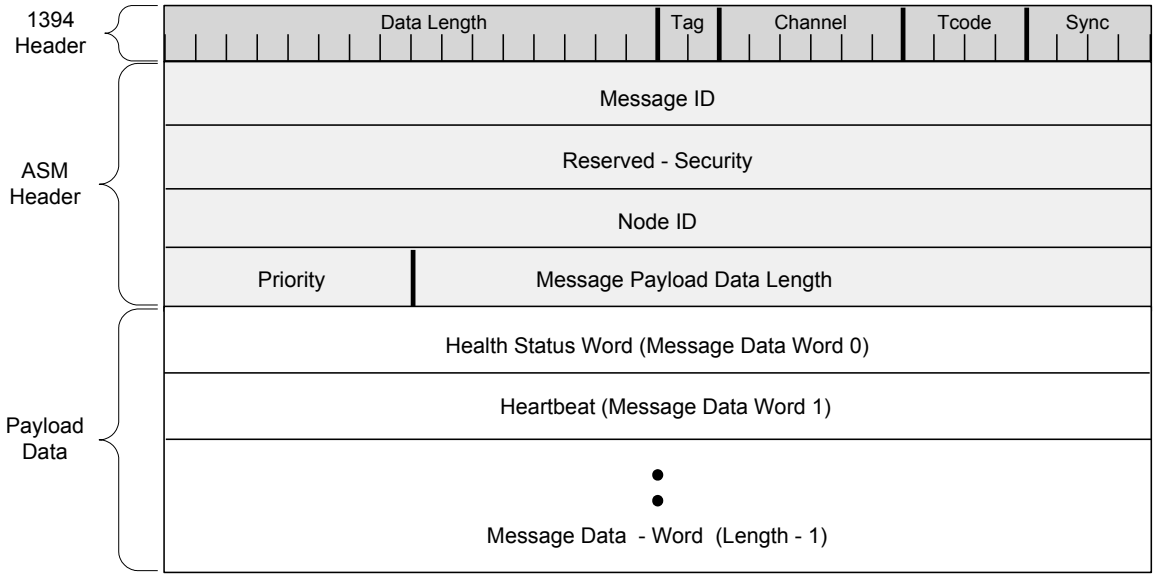

Figure 4-1: Transmit Message

4.3.2 CC Transmit Stacks

You can configure the Control Computer to use the Single-Shot Stack, the Continuous Stack, or both. The Single-Shot Stack is transmitted once, and the Continuous Stack is transmitted repeatedly. When both stacks are selected, the contents of the Single-Shot Stack are transmitted once, followed by the contents of the Continuous Stack (repeatedly).

Each stack is pointed to by a register you set. Each stack ends when an end-of-stack marker message is reached. Messages in the Single-Shot Stack are transmitted at the "initial receive offset" for the specified RN. Messages in the Continuous Stack are transmitted at the regular receive offset for the specified RN.

The messages are not sorted by the node; rather the node traverses the stack in order. To ensure that the messages go out at their proper times, put them in the stack in time order.

Table 4-33 describes the fields of each CC Transmit Stack entry.

Table 4-33: CC Transmit Stack Entry

Word	Description
0	Control Word (see below)
1	Status Word (see below)
2 – 3	32-bit pointer to the beginning of message
4 – 6	Time Tag of last actual transmission (48 bits)
7	Reserved
8	Channel number of destination RN
9	Size of message without trailer (in quadlets: the 1394 header is one quadlet, the ASM header is four quadlets, the message payload is a minimum of two quadlets, no trailer)
10 – 15	Reserved

Table 4-34 describes the fields of the CC Transmit Stack Control Word.

Table 4-34: CC Transmit Stack Control Word

Bit	Description
04 – 15	Reserved
03	Not end of stack (this bit is set to indicate that this is a real message. After the last message in the stack, insert an extra entry with this bit cleared to indicate the end of the stack.)
02	Interrupt on start of message (queuing in progress; can change the data pointer)
01	Interrupt on end of message (queuing complete; can change the data)
00	Skip this entry

Table 4-35 describes the fields of each CC Transmit Stack Status Word.

Table 4-35: CC Transmit Stack Status Word

Bit	Description
15	Message queuing complete
14	Message queuing in progress (do not change the data)
13	Message queuing beginning (do not change the data pointer)
01 – 12	reserved
00	Message error (timed out waiting for message to queue)

4.3.3 CC Linked List Area

The Linked List message area is populated with receive messages.

Table 4-36 describes the fields of each CC Linked List entry.

Table 4-36: CC Linked List Structure

Word	Description
0	Sentinel (Has three legal values (1394 (H) indicates a valid message, C1C1 (H) indicates no message, AAAA (H) indicates time to wrap around to beginning of Linked List) Any other value is illegal and probably means that you are not keeping up with the node and there was an overrun.
1	Message Status
2 – 3	Message Counter (number of messages received by node since power-up or node reset)
4 – 6	48-bit Time Tag
7 – 8	Reserved
9	Number of 16-bit words from the sentinel of this message until the next sentinel
2 words	1394 Header Word
8 words	ASM Header
Length based on payload length	Payload
8 words	Packet trailer

Note: The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

Table 4-37 describes the fields of the CC Receive Message Status Word.

Table 4-37: CC Receive Message Status Word

Bit	Description
15	Message complete
14	Message in progress
07 – 13	Reserved
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

Chapter 5 Remote Node Operation

Chapter 5 describes operation in Remote Node (RN) mode. In RN mode, the node acts as a remote node on the Bus. It transmits according to its predefined transmit STOF offset and has separate stacks for transmitting regular messages and Datapump messages. It is ready to receive data at any time during the STOF frame. Received data can be filtered by a combination of message number and transmitting RN (message type). Data blocks are configurable for each message type, with up to eight buffers per data block and a selectable buffer size. Interrupts can be requested for all messages or for specific data buffers, as well as various error conditions.

Note: When the first message from the CC assigns new offsets to a node in RN mode, the node automatically adjusts its STOF offsets.

The following topics are covered:

5.1 RN Memory Map 5-2

5.2 RN Mode Register Definitions 5-4

5.2.1 Hardware Revision Register 5-4
5.2.2 Excalibur Node ID Register 5-4
5.2.3 Interrupt Status Register 5-4
5.2.4 Interrupt Mask Register 5-5
5.2.5 Reset Time Register 5-6
5.2.6 Time Tag Registers 5-6
5.2.7 Reset Node Register 5-6
5.2.8 Transmit Message Counter Register 5-7
5.2.9 Receive Message Counter Register 5-7
5.2.10 STOF Message Counter Register 5-7
5.2.11 Receive Message Error Counter Register 5-7
5.2.12 Transmit Message Error Counter Register 5-8
5.2.13 Discarded Message Counter Register 5-8
5.2.14 Firmware Revision Register 5-8
5.2.15 Pointer to Current Entry of Transmit Stack 5-8
5.2.16 Mode Select Register 5-9
5.2.17 Start Register 5-9
5.2.18 Excalibur Node Status Register 5-9
5.2.19 Port Status Register 5-10
5.2.20 Number of Bad STOF Messages for CC Fail Register 5-12
5.2.21 1394 Node ID Register 5-12
5.2.22 Pointer to Beginning of Transmit Stack 5-12
5.2.23 Pointer to Beginning of Datapump Stack 5-12
5.2.24 Pointer to Beginning of Receive Stack 5-12
5.2.25 Pointer to End of Receive Stack 5-13
5.2.26 Speed Code Register 5-13
5.2.27 Options Register 5-13
5.2.28 STOF Period Register 5-14
5.2.29 Last STOF Message Status Register 5-14
5.2.30 Last STOF Message Area 5-15
5.2.31 Last STOF Time Tag Registers 5-15
5.2.32 Store STOF Messages Register 5-15
5.2.33 Receive STOF Offset Register 5-16
5.2.34 Transmit STOF Offset Register 5-16
5.2.35 Datapump STOF Offset Register 5-17
5.2.36 Channel Number Register 5-17
5.2.37 Receive STOF Offset In Use Register 5-17
5.2.38 Transmit STOF Offset In Use Register 5-18
5.2.39 Datapump STOF Offset In Use Register 5-18

5.2.40 Message Type Receive Control Table 5-18
5.3 Message Area 5-19
5.3.1 RN Transmit/Datapump Messages 5-19
5.3.2 RN Transmit/Datapump Message Stacks 5-20
5.3.3 RN Receive Message Stack 5-22
5.3.4 RN Receive Data Blocks 5-23

5.1 RN Memory Map

Table 5-1: RN Mode Memory Map Registers

Register Name	Byte Address	Read/Write	Page Number
Hardware Revision Register	0000 (H)	Read Only	5-4
Excalibur Node ID Register	0002 (H)	Read Only	5-4
Interrupt Status Register	0004 (H)	Read/Write (Write '1' to Clear)	5-4
Interrupt Mask Register	0008 (H)	Read/Write	5-5
Reset Time Register	000C (H)	Read/Write	5-6
Reserved	000E – 000F (H)		
Time Tag Low Register	0010 (H)	Read Only	5-6
Time Tag Middle Register	0012 (H)	Read Only	5-6
Time Tag High Register	0014 (H)	Read Only	5-6
Reserved	0016 – 0017H		
Reset Node Register	0018 (H)	Write Only	5-6
Reserved	001A – 007F (H)		
Transmit Message Counter Register	0080 (H)	Read Only	5-7
Reserved	0084 – 0087 (H)		
Receive Message Counter Register	0088 (H)	Read Only	5-7
Reserved	008C – 008F (H)		
STOF Message Counter Register	0090 (H)	Read Only	5-7
Reserved	0094 – 0098 (H)		
Receive Message Error Counter Register	0098 (H)	Read Only	5-7
Transmit Message Error Counter Register	009C (H)	Read Only	5-8
Discarded Message Counter Register	00A0 (H)	Read Only	5-8
Reserved	00A4 – 00A7 (H)		
Firmware Revision Register	00A8 (H)	Read Only	5-8
Pointer to Current Entry of Transmit Stack	00AC (H)	Read Only	5-8
Mode Select Register	00B0 (H)	Read/Write	5-9
Start Register	00B4 (H)	Read/Write	5-9
Excalibur Node Status Register	00B8 (H)	Read Only	5-9

Register Name	Byte Address	Read/Write	Page Number
Port Status Register	00BC (H)	Read Only	5-10
Reserved	00C0 – 00C3 (H)		
Number of Bad STOF Messages for CC Fail Register	00C4 (H)	Read/Write	5-12
1394 Node ID Register	00C8 (H)	Read Only	5-12
Reserved	00CC – 00CF (H)		
Pointer to Beginning of Transmit Stack	00D0 (H)	Read/Write	5-12
Reserved	00D4 (H)		
Pointer to Beginning of Datapump Stack	00D8 (H)	Read/Write	5-12
Reserved	00DC – 00DF (H)		
Pointer to Beginning of Receive Stack	00E0 (H)	Read/Write	5-12
Pointer to End of Receive Stack	00E4 (H)	Read/Write	5-13
Reserved	00E8 – 00EF (H)		
Speed Code Register	00F0 (H)	Read/Write	5-13
Reserved	00F2 – 00F3 (H)		
Options Register	00F4 – 00F7 (H)	Read Only	5-13
Reserved	00F8 – 00FF (H)		
STOF Period Register	0100 (H)	Read/Write	5-14
Last STOF Message Status Register	0102 (H)	Read/Write	5-14
Last STOF Message Area	0104 (H)	Read Only	5-15
Last STOF Time Tag Registers	0130 (H)	Read Only	5-15
Reserved	0136 – 0137 (H)		
Store STOF Messages Register	0138 (H)	Read/Write	5-15
Reserved	013A – 02FF (H)		
Receive STOF Offset Register	0300 (H)	Read/Write	5-17
Transmit STOF Offset Register	0304 (H)	Read/Write	5-16
Datapump STOF Offset Register	0308 (H)	Read/Write	5-16
Channel Number Register	030C (H)	Read/Write	5-17
Receive STOF Offset In Use Register	0310 (H)	Read Only	5-17
Transmit STOF Offset In Use Register	0314 (H)	Read Only	5-18
Datapump STOF Offset In Use Register	0318 (H)	Read Only	5-18
Reserved	031C – 12FF (H)		
Message Type Receive Control Table	1300 – 13EFF (H)	Read/Write	5-18
Message Area	13F00 – 1FFFFF (H)	Read/Write	5-19

5.2 RN Mode Register Definitions

5.2.1 Hardware Revision Register

Address: 0000 (H) Length: 16 bits

Read Only

This register contains the revision number of the hardware logic. 12 bits are used for the major revision, and four bits are used for the minor revision. For example, for hardware revision 2.1, 2 is stored in the high 12 bits, and 1 is stored in the low four bits.

5.2.2 Excalibur Node ID Register

Address: 0002 (H) Length: 16 bits

Read Only

This register contains the identifier of the Excalibur Node. This is set to 1394 (H).

5.2.3 Interrupt Status Register

Address: 0004 (H) Length: 32 bits

Read/Write (Write '1' to Clear)

This register indicates the occurrence various interrupt events or conditions. Each bit indicates the occurrence of a specific event/condition. The bits in this register are lit when the event/condition occurs, regardless of whether the event/condition is set to generate an interrupt. For information on generating interrupts, see the Interrupt Mask Register on page 5-5.

Table 5-2: Interrupt Status Register

Bit	Description
31	Interrupt occurred on start of message (transmit) for a specific message (queuing in progress; can change the data pointer). Check Stack Status Words for which message.
30	Interrupt occurred on end of message (transmit) for a specific message (queuing complete; can change the data). Check Stack Status Words for which message.
29	Interrupt occurred on end of message (receive) for a specific message. Check Buffer Or Receive Stack Status Words for which message.
07 – 28	Reserved
06	STOF receive complete
05	End of message queuing (transmit)
04	Start of message (transmit)
03	End of message (receive)
02	CC recognized as failed
01	Network Bus Mode changed
00	Message error

5.2.4 Interrupt Mask Register

Address: 0008 (H) Length: 32 bits

Read/Write

Use this register to set interrupts. Each bit is a flag that enables or disables the generation of a specific interrupt.

When an interrupt is received, check the Interrupt Status Register to see which condition (or conditions) caused the interrupt.

Table 5-3: Interrupt Mask Register

Bit	Description
07 – 31	Reserved
06	Interrupt on end of STOF receive
05	Interrupt on end of Transmit Stack message
04	Interrupt on start of Transmit Stack message
03	Interrupt on end of received message
02	Interrupt when CC recognized as failed
01	Interrupt when Network Bus Mode changes
00	Interrupt on message error

5.2.5 Reset Time Register

Address: 000C (H) Length: 16 bits

Read/Write

Use this register to reset the node's Time Tag.

Table 5-4: Reset Time Register

Bit	Description
01 – 15	Reserved
00	Reset Time Tag (Resets the Time Tag to 0. All message Time Tags, STOF offsets and STOF timing are based on this Time Tag value)

5.2.6 Time Tag Registers

Address: 0010 (H) Length: 48 bits

Read Only

These three registers represent the current value of the Time Tag. All message Time Tags, STOF offsets and STOF timing are based on this Time Tag value. The Time Tag has a precision of 100 nanoseconds per bit. The Time Tag should be read from address 10 then 12 then 14. When reading address 10 the Time Tag registers are frozen, reading address 14 unfreezes them.

Table 5-5: Time Tag Registers

Address	Description
10	Low 16 bits of Time Tag
12	Middle 16 bits of Time Tag
14	High 16 bits of Time Tag

5.2.7 Reset Node Register

Address: 0018 (H) Length: 16 bits

Write Only

Use this register to reset the node.

Table 5-6: Reset Node Register

Bit	Description
01 – 15	Reserved
00	Reset Node (resets the node, clears the control registers and resets the Time Tag)

5.2.8 Transmit Message Counter Register

Address: 0080 (H) Length: 32 bits

Read Only

This register contains a running counter of all messages transmitted by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 5-7: Transmit Message Counter Register

Bit	Description
00 – 31	Number of messages transmitted by the node

5.2.9 Receive Message Counter Register

Address: 0088 (H) Length: 32 bits

Read Only

This register contains a running count of all messages received and stored by the node. It does not include STOF messages which are counted separately. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 5-8: Receive Message Counter Register

Bit	Description
00 – 31	Number of messages received and stored by the node

5.2.10 STOF Message Counter Register

Address: 0090 (H) Length: 32 bits

Read Only

This register contains a running count of all STOF messages received by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 5-9: STOF Message Counter Register

Bit	Description
00 – 31	Number of STOF messages received by the node

5.2.11 Receive Message Error Counter Register

Address: 0098 (H) Length: 32 bits

Read Only

This register contains a running count of all messages with errors received and stored. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 5-10: Receive Message Error Counter Register

Bit	Description
00 – 31	Number of messages with errors received and stored by the node

5.2.12 Transmit Message Error Counter Register

Address: 009C (H) Length: 32 bits

Read Only

This register contains a running count of all transmit messages with errors. It is reset to 0 upon power-up, node reset and when the node is started.

Table 5-11: Transmit Message Error Counter Register

Bit	Description
00 – 31	Number of transmit messages with errors

5.2.13 Discarded Message Counter Register

Address: 00A0 (H) Length: 32 bits

Read Only

This register contains a running count of all messages that were discarded by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 5-12: Discarded Message Counter Register

Bit	Description
00 – 31	Number of messages received and discarded by the node

5.2.14 Firmware Revision Register

Address: 00A8 (H) Length: 32 bits

Read Only

This register contains the revision number of the firmware running on the node. 16 bits are used for the major revision, and 16 bits are used for the minor revision. For example, for firmware revision 2.1, 2 is stored in the high 16 bits, and 1 is stored in the low 16 bits.

5.2.15 Pointer to Current Entry of Transmit Stack

Address: 00AC (H) Length: 32 bits

Read Only

This register contains a pointer to the location in the Transmit Stack that is currently being transmitted.

5.2.16 Mode Select Register

Address: 00B0 (H) Length: 32 bits

Read/Write

Use this register to set the operational mode of the node.

Table 5-13: Mode Select Register

Bit	Value	Description
00 – 31	0	Node was initialized, but was not yet set into an operational mode
	1	Remote Node (RN) Mode
	2	Control Computer (CC) Mode
	3	Bus Monitor Mode
	4	Asynchronous Mode

5.2.17 Start Register

Address: 00B4 (H) Length: 32 bits

Read/Write

Use this register to start and stop the operations of the node.

Table 5-14: Start Register

Bit	Description
01 – 31	Reserved
00	1 = Start Operation 0 = Stop Operation

5.2.18 Excalibur Node Status Register

Address: 00B8 (H) Length: 32 bits

Read Only

This register indicates the current status of the node. It also provides power-on self-test information.

Table 5-15: Excalibur Node Status Register

Bit	Description
31	Reserved
30	Message fragment detected (the receive FIFO had part of a message. There was probably an overrun or other technical glitch in receiving)
29	Out-of-frame message received (received a message before first STOF or after missing STOFs)
17 – 29	Reserved
16	Wrong LLC version (indicates that the link-layer chip had technical difficulties)
5 – 15	Reserved
04	1 = Running 0 = Halted
03	1 = Self Test Passed 0 = Self Test Failed
02	Reserved
01	1 = RAM test passed 0 = RAM test failed
00	1 = Ready 0 = Not ready

5.2.19 Port Status Register

Address: 00BC (H) Length: 32 bits

Read Only

This register indicates the current status of the three ports.

Table 5-16: Port Status Register

Bit	Description
24 – 31	Reserved
23	Port 0 Connected
22	Port 0 Receive OK
21	Port 0 Beta Mode
20	Port 0 Speed Bit 0
19	Port 0 Speed Bit 1
18	Port 0 Speed Bit 2
17	Port 0 Spare
16	Port 0 Spare
15	Port 1 Connected
14	Port 1 Receive OK
13	Port 1 Beta Mode
12	Port 1 Speed Bit 0
11	Port 1 Speed Bit 1
10	Port 1 Speed Bit 2
09	Port 1 Spare
08	Port 1 Spare
07	Port 2 Connected
06	Port 2 Receive OK
05	Port 2 Beta Mode
04	Port 2 Speed Bit 0
03	Port 2 Speed Bit 1
02	Port 2 Speed Bit 2
01	Port 2 Spare
00	Port 2 Spare

Table 5-17: Port Speed Bits

Speed	Bit 2	Bit 1	Bit 0
100 Mbps	0	0	0
200 Mbps	0	0	1
400 Mbps	0	1	0
Not Supported	0	1	1
Not Supported	1	0	0

5.2.20 Number of Bad STOF Messages for CC Fail Register

Address: 00C4 (H) Length: 32 bits

Read/Write

Use this register to set the number of bad STOF messages to allow without considering the CC to have failed. After this amount of bad STOF messages, the CC is given a status of failed. The value of this register reset to 3 upon power-up and node reset.

Table 5-18: Number of Bad STOF Messages for CC Fail Register

Bit	Description
00 – 31	Number of missed STOF messages to allow

5.2.21 1394 Node ID Register

Address: 00C8 (H) Length: 32 bits

Read Only

This register contains the node ID assigned automatically during bus configuration.

Table 5-19: 1394 Node ID Register

Bit	Description
00 – 31	1394 Node ID

5.2.22 Pointer to Beginning of Transmit Stack

Address: 00D0 (H) Length: 32 bits

Read/Write

Use this register to specify the beginning of the Transmit Message Stack.

5.2.23 Pointer to Beginning of Datapump Stack

Address: 00D8 (H) Length: 32 bits

Read/Write

Use this register to specify the beginning of the Datapump Message Stack.

5.2.24 Pointer to Beginning of Receive Stack

Address: 00E0 (H) Length: 32 bits

Read/Write

Use this register to specify the beginning of the Receive Message Stack.

5.2.25 Pointer to End of Receive Stack

Address: 00E4 (H) Length: 32 bits

Read/Write

Use this register to specify the last byte of the Receive Message Stack.

5.2.26 Speed Code Register

Address: 00F0 (H) Length: 16 bits

Read/Write

Use this register to select the communications speed of the node.

Table 5-20: Speed Code Register

Bit	Description
02 – 15	Reserved
00 – 01	Speed Code

Table 5-21: Speed Code Bits

Speed	Bit 1	Speed Bit 0
100 Mbps	0	0
200 Mbps	0	1
400 Mbps	1	0
Not Supported	1	1

5.2.27 Options Register

Address: 00F4 (H) Length: 32 bits

Read Only

This register contains information about the node.

Table 5-22: Options Register

Bit	Description
02 – 15	Reserved
01	1 = By default, the Vehicle Time quadlet of each STOF message is updated before transmission (in CC mode). When this bit is lit, the option to prevent updating the Vehicle Time quadlet is available; see CC Run Configuration Register on page 4-13 0 = The option to prevent updating the Vehicle Time quadlet of the STOF message before transmission is not available
00	1 = Asynchronous mode is available 0 = Asynchronous mode is not available

5.2.28 STOF Period Register

Address: 0100 (H) Length: 16 bits

Read/Write

Use this register to set the period of time (in µsec) within which the STOF is expected to be received. The value of this register defaults to 12500 upon power-up and reset.

Table 5-23: STOF Period Register

Bit	Description
00 – 15	Period in µsec to expect to receive STOF

5.2.29 Last STOF Message Status Register

Address: 0102 (H) Length: 16 bits

Read/Write

This register contains the status of the STOF message area. Check this register to see whether the data in the STOF Message area and STOF Time Tag area are consistent and to check for errors in the STOF messages.

Table 5-24: Last STOF Message Status Register

Bit	Description
15	Message complete
14	Message in progress
09 – 13	Reserved
08	Vehicle time not progressing
07	STOF timing error (early or late STOF)
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

5.2.30 Last STOF Message Area

Address: 0104 (H) Length: 11 32-bit words

Read Only

This register contains the last STOF message received by the node. When the STOF is updated the Last STOF Message Status Register is set to 0 and the Message In Progress bit is set. When the update is complete, the STOF Message Counter Register is updated, the Message In Progress bit is cleared, the Message Complete bit is set.

Table 5-25: Last STOF Message Area

Quadlet	Description
00	1394 Header Word
01	Control Computer Branch Status
02	Network Bus Mode
03	Vehicle State
04	Vehicle Time
05 – 09	Reserved
10	Vertical Parity Check

Note: The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

5.2.31 Last STOF Time Tag Registers

Address: 0130 (H) Length: 48 bits

Read Only

These three 16-bit registers represent the value of the node's Time Tag at the time the last STOF was received.

Table 5-26: Last STOF Time Tag Registers

Word	Description
0	Low 16 bits of Time Tag
1	Middle 16 bits of Time Tag
2	High 16 bits of Time Tag

5.2.32 Store STOF Messages Register

Address: 0138 (H) Length: 16 bits

Read/Write

Use this register to set whether STOF message information will be included in the Receive Message Stack. The data associated with the most recent STOF message is always placed in the Last STOF Message area, regardless of which option is selected in this register. Since some nodes may receive only one message per STOF, including

STOF messages in the stack could result in every second entry referring to a STOF message, effectively halving the number of entries available for data messages.

Table 5-27: Store STOF Messages Register

Bit	Description
01 – 15	Reserved
00	1 = include STOF messages in Message Stack 0 = Do not include STOF messages in Message Stack

5.2.33 Receive STOF Offset Register

Address: 0300 (H) Length: 32 bits

Read/Write

Use this register to select the default receive STOF offset in µsec upon starting the node. If the first message received from the Control Computer contains a newer value, the newer value will be used in all future STOF messages, instead of the value in this register.

Note: This value may be overridden by the STOF offset values in the first packet received by the RN from the CC.

Table 5-28: Receive STOF Offset Register

Bit	Description
00 – 31	Receive STOF offset

5.2.34 Transmit STOF Offset Register

Address: 0304 (H) Length: 32 bits

Read/Write

Use this register to select the default transmit STOF offset in µsec upon starting the node. If the first message received from the Control Computer contains a newer value, the newer value will be used in all future STOF messages, instead of the value in this register.

Note: This value may be overridden by the STOF offset values in the first packet received by the RN from the CC.

Table 5-29: Transmit STOF Offset Register

Bit	Description
00 – 31	Transmit STOF offset

5.2.35 Datapump STOF Offset Register

Address: 0308 (H) Length: 32 bits

Read/Write

Use this register to select the default Datapump STOF offset in µsec upon starting the node. If the first message received from the Control Computer contains a newer value, the newer value will be used in all future STOF messages, instead of the value in this register.

Note: This value may be overridden by the STOF offset values in the first packet received by the RN from the CC.

Table 5-30: Datapump STOF Offset Register

Bit	Description
00 – 31	Datapump STOF offset

5.2.36 Channel Number Register

Address: 030C (H) Length: 32 bits

Read/Write

Use this register to specify the channel number of the remote node the channel is to simulate. Only messages addressed to this channel number or to the STOF channel are received.

Table 5-31: Channel Number Register

Bit	Description
06 – 32	Reserved
00 – 05	Channel number

5.2.37 Receive STOF Offset In Use Register

Address: 0310 (H) Length: 32 bits

Read Only

This register contains the receive STOF offset currently in use (in µsec). When the node is started, this is the same as the Receive STOF Offset Register. If the CC updates the STOF offsets, the new value is stored in this register. See Receive STOF Offset Register on page 5-16.

Table 5-32: Receive STOF Offset In Use Register

Bit	Description
00 – 31	Receive STOF offset

5.2.38 Transmit STOF Offset In Use Register

Address: 0314 (H) Length: 32 bits

Read Only

This register contains the transmit STOF offset currently in use (in µsec). When the node is started, this is the same as the Transmit STOF Offset Register. If the CC updates the STOF offsets, the new value is stored in this register. See Transmit STOF Offset Register on page 5-16.

Table 5-33: Transmit STOF Offset In Use Register

Bit	Description
00 – 31	Transmit STOF offset

5.2.39 Datapump STOF Offset In Use Register

Address: 0318 (H) Length: 32 bits

Read Only

This register contains the Datapump STOF offset currently in use (in µsec). When the node is started, this is the same as the Datapump STOF Offset Register. If the CC updates the STOF offsets, the new value is stored in this register. See Datapump STOF Offset Register on page 5-17.

Table 5-34: Datapump STOF Offset In Use Register

Bit	Description
00 – 31	Datapump STOF offset

5.2.40 Message Type Receive Control Table

Use the Message Type Receive Control Table to filter incoming messages. Its address range is 1300 – 13EFF H. The CC branch is ignored since a given node receives all its messages from the same CC branch. 6400 entries are used. The table is indexed by source channel number and message number.

Table 5-35 describes the fields of each entry in the RN Receive Control Table.

Table 5-35: Message Type Receive Control Table

Word	Description	Read/Write
0	Control Word	Write
1	Reserved	N/A
2 – 3	32 bit pointer to data block	Write
4 – 5	Reserved	N/A

Table 5-36 describes the Receive Control Table Control Word.

Table 5-36: Control Word

Bit	Description Table
1 – 15	Reserved
0	Store (1)/Do not store (0)

Note: Ensure that there is no overlap when laying out the data blocks.

5.3 Message Area

The RN Message Area contains:

- RN Transmit/Datapump Messages
- RN Transmit/Datapump Message Stacks
- RN Receive Message Stack
- RN Receive Data Blocks

Its address range is 13900 – 1FFFFF.

5.3.1 RN Transmit/Datapump Messages

Table 5-37 describes the fields in each Transmit/Datapump message.

Table 5-37: RN Message Data Area

Word	Description
0 – 1	1394 Header quadlet
2 – 9	ASM Header
Length based on payload length	Payload

Note: The data area must not contain the header CRC, the data CRC or the trailer. The trailer is comprised of the three STOF offsets and the VPC, and is automatically generated by the firmware based on the values in the STOF Offsets Table.

Figure 5-1 shows the information that you must supply in a Transmit Message.

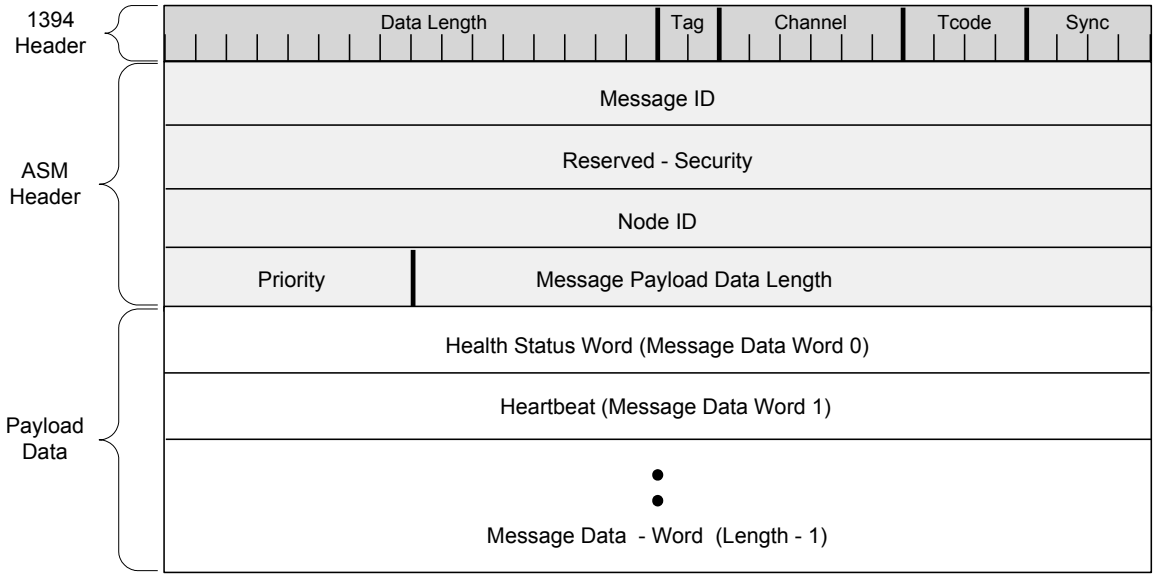

Figure 5-1: Transmit Message

5.3.2 RN Transmit/Datapump Message Stacks

In RN mode, most of the 2 MB Dual Port RAM is available for storing receive and transmit messages. The buffers are variable in size. A Transmit Message Stack enables you to schedule several messages to be transmitted in each STOF interval.

There are two stacks, one used at transmit STOF offset and one at Datapump STOF offset.

The beginning of the Transmit Message Stack is defined by the Pointer to Beginning of Transmit Stack (on page 5-12). The end of the stack is defined by the first message that has the "Not end of stack" bit cleared. Messages in the Transmit Stack are transmitted according to the remote node's transmit offset.

An identical stack is used to schedule Datapump messages. The beginning of the Datapump Message Stack is defined by the Pointer to Beginning of Datapump Stack (on page 5-12). The end of the stack is defined by the first message that has the "Not end of stack" bit cleared. Messages in the Datapump Stack are transmitted according to the remote node's Datapump offset.

Table 5-38 describes the fields in each transmission stack entry.

Table 5-38: RN Transmit/Datapump Stack Entry

Word	Description
0	Control Word (see below)
1	Status Word (see below)
2 – 3	32-bit pointer to data buffer
4 – 6	Time Tag of last actual transmission (48 bits)
7 – 8	Reserved
9	Buffer size
10 – 11	Message Counter – number of times this message has been sent
12 – 15	Reserved

Table 5-39 describes the fields of the RN Transmit Stack Entry Control Word.

Table 5-39: RN Transmit Stack Entry Control Word

Bit	Description
04 – 15	Reserved
03	Not end of stack (this bit is set to indicate that this is a real message. After the last message in the stack, insert an extra entry with this bit cleared to indicate the end of the stack.)
02	Interrupt on start of transmission (queuing)
01	Interrupt on end of transmission (queuing)
00	Skip this entry

Note that the interrupts in the Control Word are reflected in bits 30 and 31 of the Interrupt Status Register. See Interrupt Status Register on page 5-4.

Table 5-40 describes the fields of the RN Transmit Stack Status Word.

Table 5-40: RN Transmit Stack Entry Status Word

Bit	Description
15	Message queuing complete
14	Message queuing in progress (do not change the data)
13	Message queuing beginning (do not change the data pointer)
01 – 12	reserved
00	Message error (timed out waiting for message to queue)

Note: Ensure that the total transmission length of a frame does not exceed the transmit STOF offset time allocation.

5.3.3 RN Receive Message Stack

The Receive Message Stack describes the last *x* number of messages received by the node. The number of messages stored in the stack is determined by the Pointer to Beginning of Receive Stack and the Pointer to End of Receive Stack. See page 5-12.

The actual message data is not stored in the stack. The message data is stored in the RN Receive Data Blocks. See RN Receive Data Blocks on page 5-23.

STOF messages are only included the Receive Message Stack when the Store STOF Messages Register is set to Store.

Table 5-41 describes the RN Receive Message Stack.

Table 5-41: RN Receive Message Stack

Word	Description
0	Status
1	Message identifier – sending channel (bits 0 – 6) + message number (bits 7 – 13) STOF indicator is Bit 15
2 – 3	1394 Header Word
4 – 6	48-bit Time Tag
7	Reserved

Table 5-42 describes the fields of the RN Receive Message Stack Status Word.

Table 5-42: RN Receive Message Stack Status Word

Bit	Description
15	Message complete
14	Message in progress
09 – 13	Reserved
08	Vehicle time not progressing
07	STOF timing error (early or late STOF)
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

Note: Bits 7 and 8 are STOF message errors.

5.3.4 RN Receive Data Blocks

Each data block contains a header area and up to eight fixed-size data buffers. Each buffer contains a Buffer Status Word followed by the 1394 header followed by the message data (including ASM header and packet trailer).

Figure 5-2 shows the contents of an RN Receive Data Block.

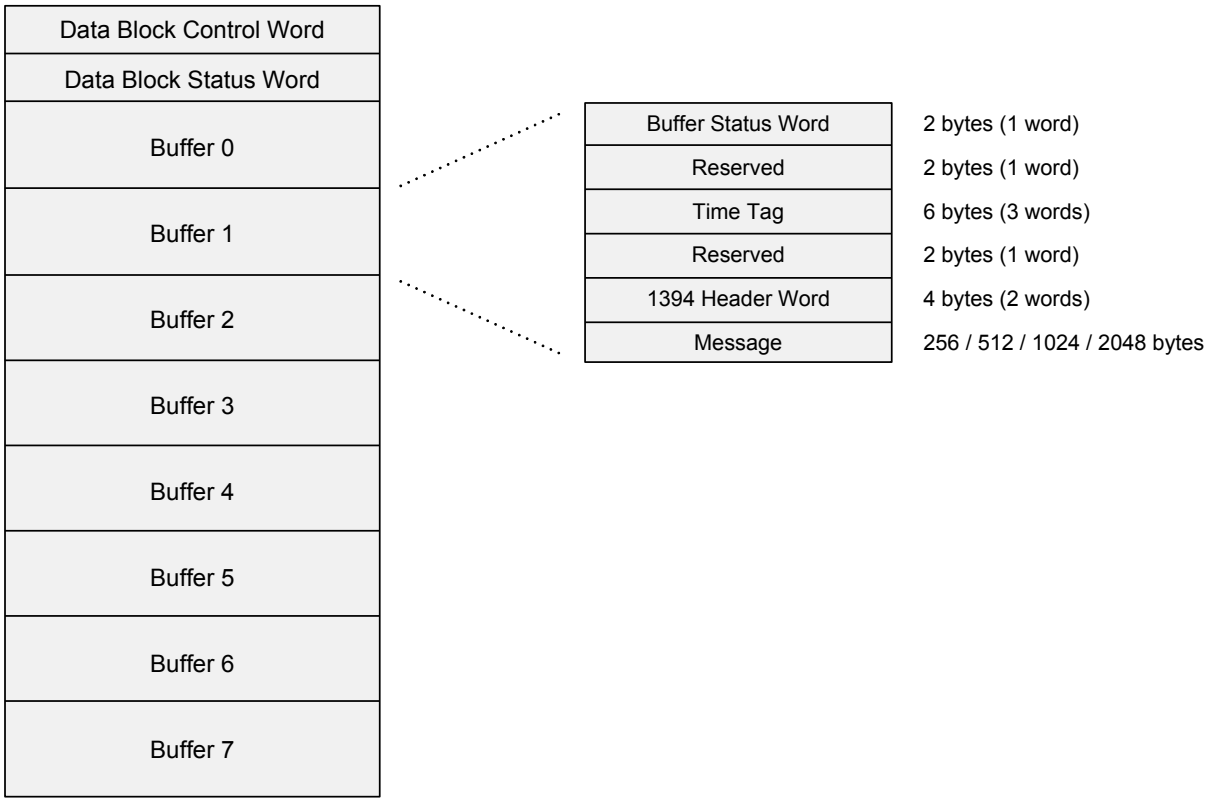

Figure 5-2: RN Receive Data Block

Note: The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

Accessing the Buffers

It is possible that during the process of freezing the desired buffer, the desired buffer became the active buffer. It is also possible that that buffer is currently being written to.

To avoid data integrity problems in these cases, do the following:

1. After freezing the desired buffer, recheck the active buffer.
2. If the desired buffer has become the active buffer, check the Buffer Status Word of that buffer to make sure it is not in the progress of being written to. See Buffer Status Word on page 5-27.
3. If the buffer is in the progress of being written to, do not read the buffer.
   If the buffer is not in the progress of being written to, (but the buffer that you froze is the active buffer), it is not recommended to read from that buffer. Instead, unfreeze the buffer and read a different buffer. However, reading the buffer will not cause problems with data integrity.

   If the buffer is frozen when the node tries to write to it, the data is written to the previous buffer and the message in the previous buffer is overwritten. If you are only using one buffer, all incoming messages are discarded until you unfreeze the buffer.
4. Read and check the Buffer Status Word. See Buffer Status Word on page 5-27.
5. Read the buffer.
6. After reading the buffer, unfreeze the buffer.

Table 5-43 describes the fields of the receive data block header.

Table 5-43: Data Block Header

Word	Description
0	Data Block Control Word
1	Data Block Status Word

Table 5-44 describes the fields of the Data Block Buffer Header Control Word.

Table 5-44: Data Block Header Control Word

Bit	Description
13 – 15	Reserved
11 – 12	Buffer size (256, 512, 1K, or 2K; plus 16 bytes for the first 8 words of the Data Block Buffer. This header information is not part of the 1394 message payload); see Table 5-45 and Table 5-47.
08 – 10	Number of buffers (0 = 1 buffer, 1 = 2 buffers, through 7 = 8 buffers)
07	Interrupt on end of message
04 – 06	Reserved
03	Freeze buffer (Boolean)
00 – 02	Buffer to freeze (0 – 7)

Note that the interrupt on end of message which can be set here is reflected in the Interrupt Status Register, Bit 29.

Table 5-45 describes the buffer size bits.

Table 5-45: Buffer Size Bits

Buffer size	Message size (bytes)	Buffer size bits	
		Bit 12 (of the Header Control Word)	Bit 11 (of the Header Control Word)
272	256	0	0
528	512	0	1
1040	1024	1	0
2064	2048	1	1

Table 5-46 describes the fields of the Receive Data Block Status Word.

Table 5-46: Data Block Header Status Word

Bit	Description
15	Message in progress
14	No unfrozen buffer when message received – message discarded
03 – 13	Reserved
00 – 02	Currently active buffer (0 – 7)

Table 5-47 describes the remote node receive data buffer.

Table 5-47: Data Block Buffer

Word	Description
0	Buffer Status Word – see Table 5-48
1	Reserved
2 – 4	Time Tag of message
5	Reserved
6 – 7	1394 Header quadlet
8 – 15	ASM header
Length based on payload length	Payload
8 words	Packet trailer

Note: The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

Table 5-48 describes the fields of the Buffer Status Word.

Table 5-48: Buffer Status Word

Bit	Description
15	Message complete
14	Message in progress
13	Buffer had to be overwritten because a message came in when the subsequent buffer would have been the active buffer but was frozen; see Accessing the Buffers on page 5-24
07 – 12	Reserved
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

Chapter 6 Asynchronous Operation

Chapter 6 describes operation in Asynchronous mode. Asynchronous mode is a simple command-response mode. In this mode, after sending a message, the node will not send another message until a response is received or the timeout period defined for the message has passed.

The one exception is an Asynchronous Stream message. When sending an Asynchronous Stream message, the node does not wait for a response and another message can be transmitted immediately.

To check for a new receive message, check the Asynchronous Receive Message Area. To make sure the receive message is in response to the latest transmit message, make sure the Time Tag is later than the transmit message, or read the Status byte of the receive message, and clear the Status byte after each time you read it.

The following topics are covered:

6.1 Asynchronous Memory Map 6-2

6.2 Asynchronous Mode Register Definitions 6-3

6.2.1 Hardware Revision Register 6-3
6.2.2 Excalibur Node ID Register 6-3
6.2.3 Interrupt Status Register 6-3
6.2.4 Interrupt Mask Register 6-4
6.2.5 Reset Time Register 6-5
6.2.6 Time Tag Registers 6-5
6.2.7 Receive Message Counter Register 6-5
6.2.8 Receive Message Error Counter Register 6-6
6.2.9 Discarded Message Counter Register 6-6
6.2.10 Firmware Revision Register 6-6
6.2.11 Mode Select Register 6-6
6.2.12 Start Register 6-7
6.2.13 Excalibur Node Status Register 6-7
6.2.14 Port Status Register 6-9
6.2.15 Options Register 6-10

6.3 Message Area 6-11

6.3.1 Asynchronous Transmit Message Areas 6-11
6.3.2 Asynchronous Receive Message Area 6-14

6.1 Asynchronous Memory Map

Table 6-1: RN Mode Memory Map Registers

Register Name	Byte Address	Read/Write	Page Number
Hardware Revision Register	0000 (H)	Read Only	6-3
Excalibur Node ID Register	0002 (H)	Read Only	6-3
Interrupt Status Register	0004 (H)	Read/Write (Write '1' to Clear)	6-3
Interrupt Mask Register	0008 (H)	Read/Write	6-4
Reset Time Register	000C (H)	Read/Write	6-5
Reserved	000E – 000F (H)		
Time Tag Low Register	0010 (H)	Read Only	6-5
Time Tag Middle Register	0012 (H)	Read Only	6-5
Time Tag High Register	0014 (H)	Read Only	6-5
Reserved	0016 – 0087 (H)		
Receive Message Counter Register	0088 (H)	Read Only	6-5
Reserved	008C – 0097 (H)		
Receive Message Error Counter Register	0098 (H)	Read Only	6-6
Reserved	009C - 009F (H)		
Discarded Message Counter Register	00A0 (H)	Read Only	6-6
Reserved	00A4 – 00A7 (H)		
Firmware Revision Register	00A8 (H)	Read Only	6-6
Reserved	00AC – 008F (H)		
Mode Select Register	00B0 – 00AF (H)	Read/Write	6-6
Start Register	00B4 (H)	Read/Write	6-7
Excalibur Node Status Register	00B8 (H)	Read Only	6-7
Port Status Register	00BC (H)	Read Only	6-9
Reserved	00C0 – 00F3 (H)		
Options Register	00F4 – 00F7 (H)	Read Only	6-10
Reserved	00F8 – 0FFF (H)		
Asynchronous Transmit Message Area	1000 – 181F (H)	Read/Write	6-11
Reserved	1820 – 2FFF (H)		
Asynchronous Receive Message Area	3000 – 380F (H)	Read	6-14
Reserved	3810 – 0FFF (H)		
Asynchronous Stream Transmit Message Area	5000 – 581F (H)	Read/Write	6-11
Reserved	5820 – 1FFFFF (H)		

6.2 Asynchronous Mode Register Definitions

6.2.1 Hardware Revision Register

Address: 0000 (H) Length: 16 bits

Read Only

This register contains the revision number of the hardware logic. 12 bits are used for the major revision, and four bits are used for the minor revision. For example, for hardware revision 2.1, 2 is stored in the high 12 bits, and 1 is stored in the low four bits.

6.2.2 Excalibur Node ID Register

Address: 0002 (H) Length: 16 bits

Read Only

This register contains the identifier of the Excalibur Node. This is set to 1394 (H).

6.2.3 Interrupt Status Register

Address: 0004 (H) Length: 32 bits

Read/Write (Write '1' to Clear)

This register indicates the occurrence various interrupt events or conditions. Each bit indicates the occurrence of a specific event/condition. The bits in this register are lit when the event/condition occurs, regardless of whether the event/condition is set to generate an interrupt. For information on generating interrupts, see the Interrupt Mask Register on page 6-5.

Table 6-2: Interrupt Status Register

Bit	Description
31	Interrupt occurred on start of message (transmit) for a specific message (queuing in progress; can change the data pointer). Check Stack Status Words for which message.
30	Interrupt occurred on end of message (transmit) for a specific message (queuing complete; can change the data). Check Stack Status Words for which message.
29	Interrupt occurred on end of message (receive) for a specific message. Check Buffer Or Receive Stack Status Words for which message.
07 – 28	Reserved
06	STOF receive complete
05	End of message queuing (transmit)
04	Start of message (transmit)
03	End of message (receive)
02	CC recognized as failed
01	Network Bus Mode changed
00	Message error

6.2.4 Interrupt Mask Register

Address: 0008 (H) Length: 32 bits

Read/Write

Use this register to set interrupts. Each bit is a flag that enables or disables the generation of a specific interrupt.

When an interrupt is received, check the Interrupt Status Register to see which condition (or conditions) caused the interrupt.

Table 6-3: Interrupt Mask Register

Bit	Description
07 – 31	Reserved
06	Interrupt on end of STOF receive
05	Interrupt on end of Transmit Stack message
04	Interrupt on start of Transmit Stack message
03	Interrupt on end of received message
02	Interrupt when CC recognized as failed
01	Interrupt when Network Bus Mode changes
00	Interrupt on message error

6.2.5 Reset Time Register

Address: 000C (H) Length: 16 bits

Read/Write

Use this register to reset the node's Time Tag.

Table 6-4: Reset Time Register

Bit	Description
01 – 15	Reserved
00	Reset Time Tag (Resets the Time Tag to 0. All message Time Tags, STOF offsets and STOF timing are based on this Time Tag value)

6.2.6 Time Tag Registers

Address: 0010 (H) Length: 48 bits

Read Only

These three registers represent the current value of the Time Tag. The Time Tag has a precision of 100 nanoseconds per bit. The Time Tag should be read from address 10 then 12 then 14. When reading address 10 the Time Tag registers are frozen, reading address 14 unfreezes them.

Table 6-5: Time Tag Registers

Address	Description
10	Low 16 bits of Time Tag
12	Middle 16 bits of Time Tag
14	High 16 bits of Time Tag

6.2.7 Receive Message Counter Register

Address: 0088 (H) Length: 32 bits

Read Only

This register contains a running count of all messages received and stored by the node. It does not include STOF messages which are counted separately. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 6-6: Receive Message Counter Register

Bit	Description
00 – 31	Number of messages received and stored by the node

6.2.8 Receive Message Error Counter Register

Address: 0098 (H) Length: 32 bits

Read Only

This register contains a running count of all messages with errors received and stored. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 6-7: Receive Message Error Counter Register

Bit	Description
00 – 31	Number of messages with errors received and stored by the node

6.2.9 Discarded Message Counter Register

Address: 00A0 (H) Length: 32 bits

Read Only

This register contains a running count of all messages that were discarded by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 6-8: Discarded Message Counter Register

Bit	Description
00 – 31	Number of messages received and discarded by the node

6.2.10 Firmware Revision Register

Address: 00A8 (H) Length: 32 bits

Read Only

This register contains the revision number of the firmware running on the node. 16 bits are used for the major revision, and 16 bits are used for the minor revision. For example, for firmware revision 2.1, 2 is stored in the high 16 bits, and 1 is stored in the low 16 bits.

6.2.11 Mode Select Register

Address: 00B0 (H) Length: 32 bits

Read/Write

Use this register to set the operational mode of the node.

Table 6-9: Mode Select Register

Bit	Value	Description
00 – 31	0	Node was initialized, but was not yet set into an operational mode
	1	Remote Node (RN) Mode
	2	Control Computer (CC) Mode
	3	Bus Monitor Mode
	4	Asynchronous Mode

6.2.12 Start Register

Address: 00B4 (H) Length: 32 bits

Read/Write

Use this register to start and stop the operations of the node.

Table 6-10: Start Register

Bit	Description
01 – 31	Reserved
00	1 = Start Operation 0 = Stop Operation

6.2.13 Excalibur Node Status Register

Address: 00B8 (H) Length: 32 bits

Read Only

This register indicates the current status of the node. It also provides power-on self-test information.

Table 6-11: Excalibur Node Status Register

Bit	Description
31	Reserved
30	Message fragment detected (the receive FIFO had part of a message. There was probably an overrun or other technical glitch in receiving)
29	Out-of-frame message received (received a message before first STOF or after missing STOFs)
17 – 29	Reserved
16	Wrong LLC version (indicates that the link-layer chip had technical difficulties)
5 – 15	Reserved
04	1 = Running 0 = Halted
03	1 = Self Test Passed 0 = Self Test Failed
02	Reserved
01	1 = RAM test passed 0 = RAM test failed
00	1 = Ready 0 = Not ready

6.2.14 Port Status Register

Address: 00BC (H) Length: 32 bits

Read Only

This register indicates the current status of the three ports.

Table 6-12: Port Status Register

Bit	Description
24 – 31	Reserved
23	Port 0 Connected
22	Port 0 Receive OK
21	Port 0 Beta Mode
20	Port 0 Speed Bit 0
19	Port 0 Speed Bit 1
18	Port 0 Speed Bit 2
17	Port 0 Spare
16	Port 0 Spare
15	Port 1 Connected
14	Port 1 Receive OK
13	Port 1 Beta Mode
12	Port 1 Speed Bit 0
11	Port 1 Speed Bit 1
10	Port 1 Speed Bit 2
09	Port 1 Spare
08	Port 1 Spare
07	Port 2 Connected
06	Port 2 Receive OK
05	Port 2 Beta Mode
04	Port 2 Speed Bit 0
03	Port 2 Speed Bit 1
02	Port 2 Speed Bit 2
01	Port 2 Spare
00	Port 2 Spare

Table 6-13: Port Speed Bits

Speed	Bit 2	Bit 1	Bit 0
100 Mbps	0	0	0
200 Mbps	0	0	1
400 Mbps	0	1	0
Not Supported	0	1	1
Not Supported	1	0	0

6.2.15 Options Register

Address: 00F4 (H) Length: 32 bits

Read Only

This register contains information about the node.

Table 6-14: Options Register

Bit	Description
02 – 15	Reserved
01	1 = By default, the Vehicle Time quadlet of each STOF message is updated before transmission (in CC mode). When this bit is lit, the option to prevent updating the Vehicle Time quadlet is available; see CC Run Configuration Register on page 4-13 0 = The option to prevent updating the Vehicle Time quadlet of the STOF message before transmission is not available
00	1 = Asynchronous mode is available 0 = Asynchronous mode is not available

6.3 Message Area

The Asynchronous mode has:

- Asynchronous Transmit Message Area
- Asynchronous Stream Transmit Message Area
- Asynchronous Receive Message Area

6.3.1 Asynchronous Transmit Message Areas

There are two Transmit Message areas:

- The Asynchronous Transmit Message Area is located at 1000 – 181F (H). This area is for all Asynchronous messages except for Asynchronous Stream messages.
- The Asynchronous Stream Transmit Message Area is located at 5000 – 581F (H). This area is for Asynchronous Stream messages.

Both Transmit Message areas have the same structure. There are three main sections:

- Handshake Register Area – The data in these registers is necessary to communicate with the firmware, but are not transmitted with the message.
- 1394 Header – The 1394 Header is transmitted with the message.
- Data Area – The Data Area is transmitted with the message. Its contents vary depending on the type of Asyncronous message.

Note: The data area must not contain the header CRC or the data CRC. They are automatically generated by the firmware.

Tables 6-15 through 6-19 list the information related to a transmit message. This information is comprised of:

- Transmit Handshake Registers
- 1394 Header and Data Area

The Transmit Handshake Registers are described in Table 6-15. Words 5 and 6 of the Transmit Handshake Registers (message size and receive timeout) are supplied by the user when creating the transmit message. Word 0 (Control Word) is supplied by the user to notify the firmware that a transmit message is ready to be sent. Words 2 – 4 (Time Tag) are supplied by the firmware at the time that the message is queued for transmission. Words 1 and 7 (Status Word and Ack code) are supplied by the firmware when the a message is received in response or the timeout period was reached.

Table 6-15: Transmit Handshake Registers

Word	Description
0	Control Word (see Table 6-16 on page 6-12)
1	Status Word (see Table 6-17 on page 6-12)
2 – 4	Time Tag of transmission (48 bits)
5	Size of message in quadlets including message header
6	Receive timeout in milliseconds
7	5-bit Ack code (4 bits from the standard + 1 bit of extra information (see Table 6-18 on page 6-13)
8 – 15	Reserved

Table 6-16: Control Word Bits

Bit	Description
15	Fresh data
00 – 14	Reserved

Table 6-17: Status Word Bits

Bit	Description
15	Message queuing complete
14	Message queuing in progress
01 – 13	Reserved
00	Message error (timed out waiting for message to queue)

Table 6-18: Ack Codes

Ack Code	Name
00000	Reserved
00001	Ack_complete
00010	Ack_pending
00011	Reserved
00100	Ack_busy_X
00101	Ack_busy_A
00110	Ack_busy_B
00111 – 01010	Reserved
01011	Ack_tardy
01100	Ack_conflict_error
01101	Ack_data_error
01110	Ack_type_error
01111	Ack_address_error
10000	No ack received
Note: The following codes are added by the link layer and are not part of the IEEE 1394-1995 standard.	
10001	Ack too long (more than 8 bits)
10010	Ack too short (less than 8 bits)
10011-11111	Reserved

Table 6-19: 1394 Header and Data Area

Word	Description
0 – 3	1394 Header quadlets (see Figure 6-1)
4 – 256 (length used based on payload length)	Payload area

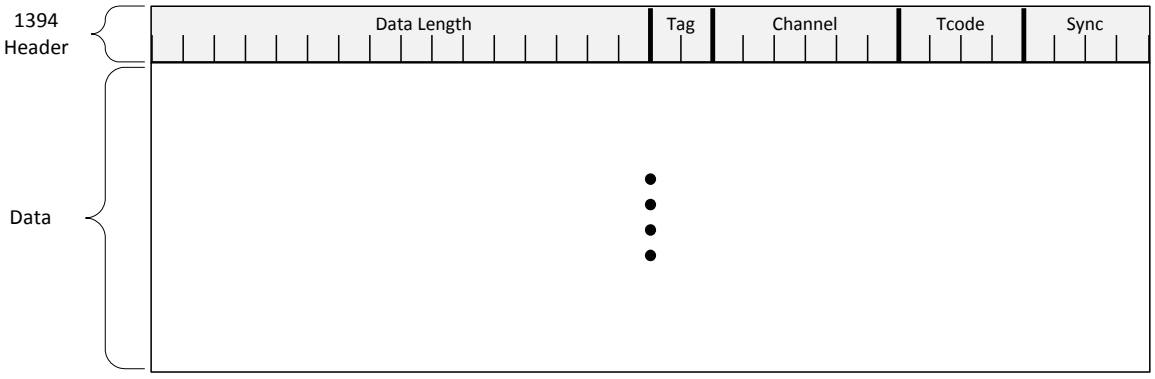

Figure 6-1: Asynchronous [Stream] Transmit Message

6.3.2 Asynchronous Receive Message Area

This register contains the last Asynchronous message received by the node. Its located at 3000 – 380F (H).

The Asynchronous Receive Message Area has three main sections:

- Receive Message Information Registers – The data in these registers is based on communicate with the firmware, but was not received with the message.
- 1394 Header – The 1394 Header that was received with the message.
- Data Area – The Data Area contains the data that was received with the message. Its contents vary depending on the type of Asyncronous message.

Note: The data area does not contain the header CRC or the data CRC.

Tables 6-20 through 6-22 list the information in a receive message.

Table 6-20: Receive Message Information Registers

Word	Description
0	Reserved
1	Status Word (see Table 6-21 on page 6-14)
2 – 4	Time Tag when the message was received (48 bits)
5	Actual quadlet count
6 – 7	Reserved

Table 6-21: Status Word Bits

Bit	Description
15	Message complete
14	Message in progress
08 – 13	Reserved
07	Timed out waiting for async response
06	Lost quadlets; some quadlets that were received on the bus were lost probably due to heavy communications traffic
05	Reserved
04	Low word count; actual length does not match the 1394 header length
03	Reserved
02	Bad CRC or high word count; actual length does not match the 1394 header length
01	Reserved
00	Message error; an error occurred, specified in one of the other bits

Table 6-22: 1394 Header and Data Area

Word	Description
0 – 3	1394 Header quadlets (see Figure 6-2)
4 – 256 (length used based on payload length)	Payload area

Figure 6-2: Asynchronous Receive Message

Chapter 7 Bus Monitor Operation

Chapter 7 describes operation in Bus Monitor mode. In Bus Monitor mode, the node receives all bus messages that pass through its ports, and stores them in memory with their timestamps. Filtering is available for storing only specific messages. Triggering is available to capture a snapshot of data surrounding a specific event. Data can be recorded either to the almost 2-MB Dual Port RAM buffer or to a 128-MB SDRAM buffer. The Dual Port RAM can be used for real time monitoring. The 128-MB SDRAM should be used in conjunction with triggering to record a large buffer relating to a specific event. 1 MB at a time can be accessed via DPRAM when the node is stopped.

The following topics are covered:

7.1 Bus Monitor Memory Map 7-2

7.2 Bus Monitor Mode Register Definitions 7-4

7.2.1 Hardware Revision Register 7-4
7.2.2 Excalibur Node ID Register 7-4
7.2.3 Interrupt Status Register 7-4
7.2.4 Interrupt Mask Register 7-5
7.2.5 Reset Time Register 7-6
7.2.6 Time Tag Registers 7-7
7.2.7 Reset Node Register 7-7
7.2.8 Receive Message Counter Register 7-7
7.2.9 STOF Message Counter Register 7-8
7.2.10 Receive Message Error Counter Register 7-8
7.2.11 Discarded Message Counter Register 7-8
7.2.12 Firmware Revision Register 7-8
7.2.13 Mode Select Register 7-9
7.2.14 Start Register 7-9
7.2.15 Excalibur Node Status Register 7-9
7.2.16 Port Status Register 7-10
7.2.17 Number of Bad STOF Messages for CC Fail Register 7-12
7.2.18 Pointer to Beginning of Receive Linked List 7-12
7.2.19 Pointer to Beginning of Receive Stack 7-12
7.2.20 Pointer to End of Receive Stack 7-12
7.2.21 Options Register 7-13
7.2.22 STOF Period Register 7-13
7.2.23 Last STOF Message Status Register 7-13
7.2.24 Last STOF Message Area 7-14
7.2.25 Last STOF Time Tag Registers 7-15
7.2.26 Store STOF Messages Register 7-15
7.2.27 Pointer to Most Recent Message 7-15
7.2.28 Pointer to Least Recent Message 7-16
7.2.29 Pointer to Trigger Message 7-16
7.2.30 Trigger Control Register 7-16
7.2.31 Trigger Position Register 7-17
7.2.32 Linked List Fill Control Register 7-18
7.2.33 Control Table Selection Register 7-18
7.2.34 STOF Offsets Control Register 7-18
7.2.35 STOF Filter Window Begin Register 7-19
7.2.36 STOF Filter Window End Register 7-19
7.2.37 Memory Select Register 7-20
7.2.38 Bank Select Register 7-20
7.2.39 Current Bank Register 7-21
7.2.40 PHY Base Registers 7-21
7.2.41 PHY Port 0 Status Registers 7-21
7.2.42 PHY Port 1 Status Registers 7-21
7.2.43 PHY Port 2 Status Registers 7-22

7.2.44 Monitor Control Tables 7-22
7.2.45 Bus Monitor STOF Offsets Table 7-23
7.2.46 Data Trigger Table 7-24
7.3 Message Area 7-26
7.3.1 Bus Monitor Receive Stack 7-26
7.3.2 Bus Monitor Linked List 7-27
7.3.3 Banked Window into SDRAM 7-31

7.1 Bus Monitor Memory Map

Table 7-1: Bus Monitor Mode Memory Map Registers

Register Name	Byte Address	Read/Write	Page Number
Hardware Revision Register	0000 (H)	Read Only	7-4
Excalibur Node ID Register	0002 (H)	Read Only	7-4
Interrupt Status Register	0004 (H)	Read/Write (Write '1' to Clear)	7-4
Interrupt Mask Register	0008 (H)	Read/Write	7-5
Reset Time Register	000C (H)	Read/Write	7-6
Reserved	000E – 000F (H)		
Time Tag Low Register	0010 (H)	Read Only	7-7
Time Tag Middle Register	0012 (H)	Read Only	7-7
Time Tag High Register	0014 (H)	Read Only	7-7
Reserved	0016 – 0017H		
Reset Node Register	0018H	Write Only	7-7
Reserved	001A – 0087 (H)		
Receive Message Counter Register	0088 (H)	Read Only	7-7
Reserved	008C – 008F (H)		
STOF Message Counter Register	0090 (H)	Read Only	7-8
Reserved	0094 – 0097 (H)		
Receive Message Error Counter Register	0098 (H)	Read Only	7-8
Reserved	009C – 009F (H)		
Discarded Message Counter Register	00A0 (H)	Read Only	7-8
Reserved	00A4 – 00A7 (H)		
Firmware Revision Register	00A8 (H)	Read Only	7-8
Reserved	00AC – 00AF (H)		
Mode Select Register	00B0 (H)	Read/Write	7-9
Start Register	00B4 (H)	Read/Write	7-9
Excalibur Node Status Register	00B8 (H)	Read Only	7-9
Port Status Register	00BC (H)	Read Only	7-10
Reserved	00C0 – 00C3 (H)		

Register Name	Byte Address	Read/Write	Page Number
Number of Bad STOF Messages for CC Fail Register	00C4 (H)	Read/Write	7-12
Reserved	00C8 – 00D7 (H)		
Pointer to Beginning of Receive Linked List	00D8 (H)	Read Only	7-12
Reserved	00DC – 00DF (H)		
Pointer to Beginning of Receive Stack	00E0 (H)	Read Only	7-12
Pointer to End of Receive Stack	00E4 (H)	Read Only	7-12
Reserved	00E8 – 00F3 (H)		
Options Register	00F4 – 00F7 (H)	Read Only	7-13
Reserved	00F8 – 00FF (H)		
STOF Period Register	0100 (H)	Read/Write	7-13
Last STOF Message Status Register	0102 (H)	Read/Write	7-13
Last STOF Message Area	0104 (H)	Read Only	7-14
Last STOF Time Tag Registers	0130 (H)	Read Only	7-15
Reserved	0136 – 0137 (H)		
Store STOF Messages Register	0138 (H)	Read/Write	7-15
Reserved	013A – 013B (H)		
Pointer to Most Recent Message	013C (H)	Read Only	7-15
Pointer to Least Recent Message	0140 (H)	Read Only	7-16
Pointer to Trigger Message	0144 (H)	Read Only	7-16
Trigger Control Register	0148 (H)	Read/Write	7-16
Trigger Position Register	014C (H)	Read/Write	7-17
Linked List Fill Control Register	014E (H)	Read/Write	7-18
Control Table Selection Register	0150 (H)	Read/Write	7-18
STOF Offsets Control Register	0152 (H)	Read/Write	7-18
STOF Filter Window Begin Register	0154 (H)	Read/Write	7-19
STOF Filter Window End Register	0158 (H)	Read/Write	7-19
Reserved	015C – 015F (H)		
Memory Select Register	0160 (H)	Read/Write	7-20
Bank Select Register	0162 (H)	Read/Write	7-20
Current Bank Register	0164 (H)	Read Only	7-21
Reserved	0166 – 0167 (H)		
PHY Base Registers	0168 – 016F (H)	Read Only	7-21
PHY Port 0 Status Registers	0170 – 0177 (H)	Read Only	7-21
PHY Port 1 Status Registers	0178 – 017F (H)	Read Only	7-21
PHY Port 2 Status Registers	0180 – 0187 (H)	Read Only	7-21
Reserved	0188 – 02FF (H)		

Register Name	Byte Address	Read/Write	Page Number
Message Type Receive Control Table	0300 – 34FF (H)	Read/Write	7-22
Source and Destination Channel Receive Control Table	3500 – 44FF (H)	Read/Write	7-22
Bus Monitor STOF Offsets Table	5500 – 5AFF (H)	Read/Write	7-23
Reserved	5B00 – 5CFF (H)		
Data Trigger Table	5D00 – 5E8F (H)	Read/Write	7-24
Reserved	5E90 – 5EEF (H)		
Message Area	5EF0 – 1FFFFF (H)		7-26

7.2 Bus Monitor Mode Register Definitions

7.2.1 Hardware Revision Register

Address: 0000 (H) Length: 16 bits

Read Only

This register contains the revision number of the hardware logic. 12 bits are used for the major revision, and four bits are used for the minor revision. For example, for hardware revision 2.1, 2 is stored in the high 12 bits, and 1 is stored in the low four bits.

7.2.2 Excalibur Node ID Register

Address: 0002 (H) Length: 16 bits

Read Only

This register contains the identifier of the Excalibur Node. This is set to 1394 (H).

7.2.3 Interrupt Status Register

Address: 0004 (H) Length: 32 bits

Read/Write (Write '1' to Clear)

This register indicates the occurrence various interrupt events or conditions. Each bit indicates the occurrence of a specific event/condition. The bits in this register are lit when the event/condition occurs, regardless of whether the event/condition is set to generate an interrupt. For information on generating interrupts, see the Interrupt Mask Register on page 7-5.

Table 7-2: Interrupt Status Register

Bit	Description
30 – 31	Reserved
29	Interrupt occurred on end of message (receive) for a specific message. Check Linked List Status Words for which message.
15 – 28	Reserved
14	End of buffer reached
13	Buffer midpoint reached
12	STOF vehicle time not incrementing
11	STOF VPC error
10	STOF timing error (missed, early, or late STOF)
09	Bus reset
08	Data trigger matched
07	STOF offset error (for more information, see the Bus Monitor STOF Offsets Table status for each channel)
06	STOF receive complete
04 – 05	Reserved
03	End of message
02	CC recognized as failed
01	Network Bus Mode changed
00	Message error

7.2.4 Interrupt Mask Register

Address: 0008 (H) Length: 32 bits

Read/Write

Use this register to set interrupts. Each bit is a flag that enables or disables the generation of a specific interrupt.

When an interrupt is received, check the Interrupt Status Register to see which condition (or conditions) caused the interrupt.

Table 7-3: Interrupt Mask Register

Bit	Description
15 – 31	Reserved
14	Interrupt on end of buffer reached
13	Interrupt on buffer midpoint reached
12	Interrupt when STOF vehicle time not incrementing
11	Interrupt on STOF VPC error
10	Interrupt on STOF timing error (missed, early, or late STOF)
09	Interrupt on bus reset
08	Interrupt on data trigger
07	Interrupt on STOF offset error
06	Interrupt on end of STOF receive
04 – 05	Reserved
03	Interrupt on end of message
02	Interrupt when CC recognized as failed
01	Interrupt when Network Bus Mode changes
00	Interrupt on message error

7.2.5 Reset Time Register

Address: 000C (H) Length: 16 bits

Read/Write

Use this register to reset the node's Time Tag.

Table 7-4: Reset Time Register

Bit	Description
01 – 15	Reserved
00	Reset Time Tag (Resets the Time Tag to 0. All message Time Tags, STOF offsets and STOF timing are based on this Time Tag value)

7.2.6 Time Tag Registers

Address: 0010 (H) Length: 48 bits

Read Only

These three registers represent the current value of the Time Tag. All message Time Tags, STOF offsets and STOF timing are based on this Time Tag value. The Time Tag has a precision of 100 nanoseconds per bit. The Time Tag should be read from address 10 then 12 then 14. When reading address 10 the Time Tag registers are frozen, reading address 14 unfreezes them.

Table 7-5: Time Tag Registers

Address	Description
10	Low 16 bits of Time Tag
12	Middle 16 bits of Time Tag
14	High 16 bits of Time Tag

7.2.7 Reset Node Register

Address: 0018 (H) Length: 16 bits

Write Only

Use this register to reset the node.

Table 7-6: Reset Node Register

Bit	Description
01 – 15	Reserved
00	Reset Node (resets the node, clears the control registers and resets the Time Tag)

7.2.8 Receive Message Counter Register

Address: 0088 (H) Length: 32 bits

Read Only

This register contains a running count of all messages received and stored by the node. It does not include STOF messages which are counted separately. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 7-7: Receive Message Counter Register

Bit	Description
00 – 31	Number of messages received and stored by the node

7.2.9 STOF Message Counter Register

Address: 0090 (H) Length: 32 bits

Read Only

This register contains a running count of all STOF messages received by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 7-8: STOF Message Counter Register

Bit	Description
00 – 31	Number of STOF messages received by the node

7.2.10 Receive Message Error Counter Register

Address: 0098 (H) Length: 32 bits

Read Only

This register contains a running count of all messages with errors received and stored. It does not include messages which did not pass the filters and thus were not saved. It is reset to 0 upon power-up, node reset and when the node is started.

Table 7-9: Receive Message Error Counter Register

Bit	Description
00 – 31	Number of messages with errors received and stored by the node

7.2.11 Discarded Message Counter Register

Address: 00A0 (H) Length: 32 bits

Read Only

This register contains a running count of all messages that were discarded by the node. It is reset to 0 upon power-up, node reset and when the node is started.

Table 7-10: Discarded Message Counter Register

Bit	Description
00 – 31	Number of messages received and discarded by the node

7.2.12 Firmware Revision Register

Address: 00A8 (H) Length: 32 bits

Read Only

This register contains the revision number of the firmware running on the node. 16 bits are used for the major revision, and 16 bits are used for the minor revision. For example, for firmware revision 2.1, 2 is stored in the high 16 bits, and 1 is stored in the low16 bits.

7.2.13 Mode Select Register

Address: 00B0 (H) Length: 32 bits

Read/Write

Use this register to select the operational mode of the node.

Table 7-11: Mode Select Register

Bit	Value	Description
00 – 31	0	Node was initialized, but was not yet set into an operational mode
	1	Remote Node (RN) Mode
	2	Control Computer (CC) Mode
	3	Bus Monitor Mode
	4	Asynchronous Mode

7.2.14 Start Register

Address: 00B4 (H) Length: 32 bits

Read/Write

Use this register to start and stop the operations of the node.

Table 7-12: Start Register

Bit	Description
01 – 31	Reserved
00	1 = Start Operation 0 = Stop Operation

7.2.15 Excalibur Node Status Register

Address: 00B8 (H) Length: 32 bits

Read Only

This register indicates the current status of the node. It also provides power-on self-test information.

Table 7-13: Excalibur Node Status Register

Bit	Description
31	Reserved
30	Message fragment detected (the receive FIFO had part of a message. There was probably an overrun or other technical glitch in receiving)
29	Out-of-frame message received (received a message before first STOF or after missing STOFs)
17 – 29	Reserved
16	Wrong LLC version (indicates that the link-layer chip had technical difficulties)
05 – 15	Reserved
04	1 = Running 0 = Halted
03	1 = Self Test Passed 0 = Self Test Failed
02	Reserved
01	1 = RAM test passed 0 = RAM test failed
00	1 = Ready 0 = Not ready

7.2.16 Port Status Register

Address: 00BC (H) Length: 32 bits

Read Only

This register indicates the current status of the three ports.

Table 7-14: Port Status Register

Bit	Description
24 – 31	Reserved
23	Port 0 Connected
22	Port 0 Receive OK
21	Port 0 Beta Mode
20	Port 0 Speed Bit 0
19	Port 0 Speed Bit 1
18	Port 0 Speed Bit 2
17	Port 0 Spare
16	Port 0 Spare
15	Port 1 Connected
14	Port 1 Receive OK
13	Port 1 Beta Mode
12	Port 1 Speed Bit 0
11	Port 1 Speed Bit 1
10	Port 1 Speed Bit 2
09	Port 1 Spare
08	Port 1 Spare
07	Port 2 Connected
06	Port 2 Receive OK
05	Port 2 Beta Mode
04	Port 2 Speed Bit 0
03	Port 2 Speed Bit 1
02	Port 2 Speed Bit 2
01	Port 2 Spare
00	Port 2 Spare

Table 7-15: Port Speed Bits

Speed	Bit 2	Bit 1	Bit 0
100 Mbps	0	0	0
200 Mbps	0	0	1
400 Mbps	0	1	0
Not Supported	0	1	1
Not Supported	1	0	0

7.2.17 Number of Bad STOF Messages for CC Fail Register

Address: 00C4 (H) Length: 32 bits

Read/Write

Use this register to set the number of bad STOF messages to allow without considering the CC to have failed. After this amount, the CC has a status of failed. The value of this register reset to 3 upon power-up and node reset.

Table 7-16: Number of Bad STOF Messages for CC Fail Register

Bit	Description
00 – 31	Number of missed STOF messages to allow

7.2.18 Pointer to Beginning of Receive Linked List

Address: 00D8 (H) Length: 32 bits

Read Only

This read only register contains a pointer to the beginning of the Linked List. Use this address to access the list.

Note: This register does not contain valid data when received messages are stored in SDRAM. See Memory Select Register on page 7-20.

7.2.19 Pointer to Beginning of Receive Stack

Address: 00E0 (H) Length: 32 bits

Read Only

This register contains a pointer to the beginning of the Receive Stack. Use this address to access the stack.

Note: This register is not defined when the Linked List is in DPRAM.

7.2.20 Pointer to End of Receive Stack

Address: 00E4 (H) Length: 32 bits

Read Only

This register contains a pointer to the last byte of the Receive Stack.

7.2.21 Options Register

Address: 00F4 (H) Length: 32 bits

Read Only

This register contains information about the node.

Table 7-17: Options Register

Bit	Description
02 – 15	Reserved
01	1 = By default, the Vehicle Time quadlet of each STOF message is updated before transmission (in CC mode). When this bit is lit, the option to prevent updating the Vehicle Time quadlet is available; see CC Run Configuration Register on page 4-13 0 = The option to prevent updating the Vehicle Time quadlet of the STOF message before transmission is not available
00	1 = Asynchronous mode is available 0 = Asynchronous mode is not available

7.2.22 STOF Period Register

Address: 0100 (H) Length: 16 bits

Read/Write

Use this register to set the period of time (in µsec) within which the STOF is expected to be received. The value of this register defaults to 12500 upon power-up and reset.

Table 7-18: STOF Period Register

Bit	Description
00 – 15	Period in µsec to expect to receive STOF

7.2.23 Last STOF Message Status Register

Address: 0102 (H) Length: 16 bits

Read/Write

This register contains the status of the STOF message area. Check this register to see whether the data in the STOF Message area and STOF Time Tag area are consistent and to check for errors in the STOF messages.

Table 7-19: Last STOF Message Status Register

Bit	Description
15	Message complete
14	Message in progress
09 – 13	Reserved
08	Vehicle time not progressing
07	STOF timing error (early or late STOF)
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

7.2.24 Last STOF Message Area

Address: 0104 (H) Length: 11 32-bit words

Read Only

This register contains the last STOF message received by the node. When the STOF is updated the Last STOF Message Status Register is set to 0 and the Message In Progress bit is set. When the update is complete, the STOF Message Counter Register is updated, the Message In Progress bit is cleared, the Message Complete bit is set.

Table 7-20: Last STOF Message Area

Quadlet	Description
0	1394 Header Word
1	Control Computer Branch Status
2	Network Bus Mode
3	Vehicle State
4	Vehicle Time
5 – 9	Reserved
10	Vertical Parity Check

Note: The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

7.2.25 Last STOF Time Tag Registers

Address: 0130 (H) Length: 48 bits

Read Only

These three 16-bit registers represent the value of the node's Time Tag at the time the last STOF was received.

Table 7-21: Last STOF Time Tag Registers

Word	Description
0	Low 16 bits of Time Tag
1	Middle 16 bits of Time Tag
2	High 16 bits of Time Tag

7.2.26 Store STOF Messages Register

Address: 0138 (H) Length: 16 bits

Read/Write

Use this register to set whether STOF message information will be included in the Receive Message Stack and whether the STOF messages themselves will be included in the Linked List. The data associated with the most recent STOF message is always placed in the Last STOF Message Area, regardless of which options are selected in this register.

Table 7-22: Store STOF Messages Register

Bit	Description
02 – 15	Reserved
01	1 = include STOF messages in Linked List 0 = Do not include STOF messages in Linked List
00	1 = include STOF messages in Message Stack 0 = Do not include STOF messages in Message Stack **Note:** This is only relevant when saving the Linked List in SDRAM. When saving the Linked List to DPRAM there is no Message Stack

7.2.27 Pointer to Most Recent Message

Address: 013C (H) Length: 32 bits

Read Only

This register contains a pointer (as an offset from the beginning of DPRAM or SDRAM, depending on the option selected in the Memory Select Register) to the beginning of the last complete message received by the node.

Table 7-23: Pointer to Most Recent Message

Bit	Description
00 – 31	Pointer to sentinel of most recent message in the buffer

7.2.28 Pointer to Least Recent Message

Address: 0140 (H) Length: 32 bits

Read Only

This register contains a pointer (as an offset from the beginning of DPRAM or SDRAM, depending on the option selected in the Memory Select Register) to the beginning of the oldest complete message received by the node.

Table 7-24: Pointer to Least Recent Message

Bit	Description
00 – 31	Pointer to sentinel of the oldest message in the buffer

7.2.29 Pointer to Trigger Message

Address: 0144 (H) Length: 32 bits

Read Only

This register contains a pointer (as an offset from the beginning of DPRAM or SDRAM, depending on the option selected in the Memory Select Register) to the beginning of the message which triggered the node to halt, where such a message exists. Such a message will not exist when the node was triggered by an event, such as a bus reset, which is not related to any message. In this event, the contents of this register will be zero.

Table 7-25: Pointer to Trigger Message

Bit	Description
00 – 31	Pointer to sentinel of the message which triggered the node to stop

7.2.30 Trigger Control Register

Address: 0148 (H) Length: 32 bits

Read/Write

Use this register to set up events that will stop the node. Use this register to like an oscilloscope trigger to focus on a particular event. It is particularly useful when used in conjunction with the 128-MB SDRAM buffer since the data in SDRAM cannot be viewed in real time. Use the trigger to stop bus monitoring when the buffer contains the desired data. Use this register in conjunction with the Trigger Position Register on page 7-17.

Table 7-26: Trigger Control Register

Bit	Description
13 – 31	Reserved
12	Trigger when STOF vehicle time not incrementing
11	Trigger on STOF VPC error
10	Trigger on STOF timing error (missed, early, or late STOF)
09	Trigger on bus reset
08	Trigger on data quadlet(s) (Enable Trigger Control Table) (see Data Trigger Table on page 7-24)
07	Trigger on STOF offset error (for more information, see the Bus Monitor STOF Offsets Table status for each channel)
03 – 06	Reserved
02	Trigger when CC recognized as failed
01	Trigger when Network Bus Mode changes
00	Trigger on message error

7.2.31 Trigger Position Register

Address: 014C (H) Length: 16 bits

Read/Write

Use this register to control what the node does when a message matching a trigger is received.

Table 7-27: Trigger Position Register

Bit	Description
02 – 15	Reserved
00 – 01	0 = Trigger at beginning – when the trigger is encountered, the monitor stores one complete buffer of data, with the message that triggered as the oldest message in the buffer. 1 = Trigger at end – the monitor stores all messages until the trigger message is encountered. It stops with the trigger message being the last message in the buffer. 2 = Trigger in middle – the monitor stores all messages until the trigger message is encountered. It then continues storing messages until it fills half of the buffer. The trigger message is then in the middle of the resulting buffer.

7.2.32 Linked List Fill Control Register

Address: 014E (H) Length: 16 bits

Read/Write

Use this register to control the behavior of the node when the Linked List data buffer is full.

Table 7-28: Linked List Fill Control Register

Bit	Description
01 – 15	reserved
00	1 = Stop node when buffer is full 0 = Overwrite start of buffer when buffer is full

7.2.33 Control Table Selection Register

Address: 0150 (H) Length: 16 bits

Read/Write

Use this register to select which of the Control Tables to use.

Table 7-29: Control Table Selection Register

Bit	Description
00 – 15	0 = Do not use Control Tables 1 = Use Message ID Receive Control Table 2 = Use Source and Destination Channel Receive Control Table

7.2.34 STOF Offsets Control Register

Address: 0152 (H) Length: 16 bits

Read/Write

Use this register to turn configure STOF offsets checking. When STOF offsets checking is OFF, the Monitor Mode Bus Monitor STOF Offsets Table (on page 23) is not used. When STOF offsets checking is ON, STOF timing errors are identified. For example, it is determined whether a node transmitted at the wrong time (that is, not at its transmit offset), a node did not transmit anything at its transmit offset, the CC did not transmit to a node at its receive offset, etc.

The STOF offsets filter window limits the messages recorded to those that come in between these two offsets from the STOF message. The size and location of the window are controlled by the STOF Filter Window Begin Register and the STOF Filter Window End Register.

If your initial STOF frame has different offsets from the others and you do not want STOF offset errors reported for the first frame, use the option Ignore STOF offset errors in first STOF frame.

Table 7-30: STOF Offsets Control Register

Bit	Description
15	Use STOF offset filter window
02 – 14	Reserved
01	Ignore STOF offset errors in first STOF frame
00	Check STOF offsets

7.2.35 STOF Filter Window Begin Register

Address: 0154 (H) Length: 32 bits

Read/Write

Use this register to specify the offset (in µsec) from the STOF message, at which to begin recording messages. For more information, see the STOF Offsets Control Register on page 7-18.

Table 7-31: STOF Filter Window Begin Register

Bit	Description
00 – 31	Starting offset from STOF offset (in µsec)

7.2.36 STOF Filter Window End Register

Address: 0158 (H) Length: 32 bits

Read/Write

Use this register to specify the offset (in µsec) from the STOF message, at which to stop recording messages. For more information, see the STOF Offsets Control Register on page 7-18.

Table 7-32: STOF Filter Window End

Bit	Description
00 – 31	Ending offset from STOF (in µsec)

7.2.37 Memory Select Register

Address: 0160 (H) Length: 16 bits

Read/Write

Use this register to select whether the node records data in the Dual Port RAM buffer (close to 2 MB) or the SDRAM buffer (128 MB). Use the Dual Port RAM when real time monitoring is required. Use 128-MB SDRAM in conjunction with triggering to record a large buffer relating to a specific event.

Table 7-33: Memory Select Register

Bit	Description
01 – 15	Reserved
00	1 = 128-MB SDRAM buffer selected 0 = 2-MB DPRAM buffer selected

7.2.38 Bank Select Register

Address: 0162 (H) Length: 16 bits

Read/Write

When using SDRAM storage (see the Memory Select Register on page 7-20), use this register to gain read only access to blocks of the 128-MB SDRAM.

SDRAM cannot be accessed directly. When using this register, the node copies a 1-MB block of SDRAM to DPRAM, where it can be read. To use this register, write the desired bank number (0 – 127) to this register. The node then copies the selected block from the SDRAM to DPRAM, in addresses 100000 – 1FFFFF (H). After the contents are copied, the node writes the bank number and to the Current Bank Register, and sets Bit 15 of that register to 1, which indicates that the contents are valid. You can then read the 1-MB block of SDRAM directly from the DPRAM window.

Note: This register can only be used when the node is stopped (not monitoring).

Table 7-34: Bank Select Register

Bit	Description
07 – 15	Reserved
00 – 06	The bank number (0 to 127) you would like to access through the DPRAM window.

7.2.39 Current Bank Register

Address: 0164 (H) Length: 16 bits

Read Only

This register shows which SDRAM bank is currently displayed in the DPRAM window (100000 (H) – 1FFFFF (H)) and whether the data is valid.

Table 7-35: Current Bank Register

Bit	Description
15	1 = if bank contents are valid 0 = if bank contents are invalid (or out of date – this bit is cleared when the node is started)
07 – 14	reserved
00 – 06	If Bit 15 = 1, this field contains the bank number reflected in DPRAM addresses 100000 (H) to 1FFFFF (H).

7.2.40 PHY Base Registers

Address: 0168 (H) Length: 64 bits

Read Only

These registers contain a copy of the PHY base registers. (Since the PHY Port Status registers are copied to the node, Byte 7, which contains the Page_Select and Port_Select registers for accessing the port registers, are not required and are reserved). For more information, refer to the documentation for the Texas Instruments TSB41BA3-EP chip.

Note: All of the port status registers are accessible at the same time.

7.2.41 PHY Port 0 Status Registers

Address: 0170 (H) Length: 64 bits

Read Only

These registers contain a copy of the port status registers for Port 0. For more information, refer to the documentation for the Texas Instruments TSB41BA3-EP chip.

7.2.42 PHY Port 1 Status Registers

Address: 0178 (H) Length: 64 bits

Read Only

These registers contain a copy of the port status registers for Port 1. For more information, refer to the documentation for the Texas Instruments TSB41BA3-EP chip.

7.2.43 PHY Port 2 Status Registers

Address: 0180 (H) Length: 64 bits

Read Only

These registers contain a copy of the port status registers for Port 2. For more information, refer to the documentation for the Texas Instruments TSB41BA3-EP chip.

7.2.44 Monitor Control Tables

There are two control tables for filtering, interrupting, and triggering on subsets of messages. The active table depends upon the settings in the Control Table Selection Register on page 7-18.

Message Type Receive Control Table

This Control Table contains 6400 16-bit word entries and is indexed by source channel number and message number. It allows filtering by source channel and message number, and allows interrupts and triggers to be generated upon receipt of specific message types.

Source and Destination Channel Receive Control Table

This Control Table contains 4096 16-bit word entries and is indexed by source channel number and destination channel number. It allows filtering by message path – by any combination of source and destination channels, and it allows interrupts and triggers to be generated upon receipt of messages directed to or from a specific channel or channels.

Control Table Fields

Each Control Table entry consists of one 16-bit Control Word which controls behavior of the node upon receipt of a message.

Table 7-36 describes each entry in the Monitor Mode Receive Control Table.

Table 7-36: Monitor Mode Receive Control Table

Bit	Description
05 – 15	Reserved
04	Trigger on end of message
03	Store/Do not Store
02	Reserved
01	Interrupt on end of message
00	Reserved

When the Bus Monitor receives a message matching a Control Table entry with the trigger bit set, it acts according to the Trigger Position Register setting.

7.2.45 Bus Monitor STOF Offsets Table

For each channel number, this table contains STOF offset information. The table is indexed by channel number. The information must be filled in if you want the monitor to report timing errors. It is used to determine whether a message has come in at the right time, whether an RN is transmitting at its transmit offset, and whether the CC is transmitting to an RN at its receive offset.

Changes made while the monitor is running may only take effect when the monitor is restarted. It is recommended to make changes while the node is stopped.

Table 7-37 describes the fields in the Bus Monitor STOF Offsets Table.

Table 7-37: Bus Monitor STOF Offsets Table

Word	Description
0 – 1	Transmit offset
2	Transmit offset duration
3	Control Word
4 – 5	Receive offset
6	Receive offset duration
7	Status Word
8 – 9	Datapump offset
10	Datapump offset duration
11	Reserved

Table 7-38 describes the fields of the Bus Monitor STOF Offsets Table Control Word.

Table 7-38: Bus Monitor STOF Offsets Table Control Word

Bit	Description
15	Check offsets for this RN
12 – 14	Reserved
11	Trigger if node did not transmit at its Datapump offset (occurs at the end of the Datapump window)
10	Trigger if CC did not transmit to node at node's receive offset (occurs at the end of the receive window)
09	Trigger if CC transmitted to node at the wrong offset
08	Trigger if node did not transmit at its transmit offset (occurs at the end of the transmit window)
07	Trigger if node transmitted at wrong offset
05 – 06	Reserved
04	Interrupt if node did not transmit at its Datapump offset (occurs at the end of the Datapump window)
03	Interrupt if CC did not transmit to node at node's receive offset (occurs at the end of the receive window)
02	Interrupt if CC transmitted to node at the wrong offset
01	Interrupt if node did not transmit at its transmit offset (occurs at the end of the transmit window)
00	Interrupt if node transmitted at wrong offset

Table 7-39 describes the fields of the Bus Monitor STOF Offsets Table Status Word.

Table 7-39: Bus Monitor STOF Offsets Table Status Word

Bit	Description
05 – 15	Reserved
04	Node did not transmit at its Datapump offset
03	CC did not transmit to node at node's receive offset
02	CC transmitted to node at the wrong offset
01	Node did not transmit at its transmit offset
00	Node transmitted at wrong offset

7.2.46 Data Trigger Table

The Data Trigger Table can contain up to 20 data trigger definitions. Each trigger has a Control Word (allowing the trigger to be marked on or off), and a Status Word, which indicates whether the trigger was triggered.

This table is read once, when Monitor mode is started. Changes made while running will only take effect when the monitor is stopped and restarted.

Trigger on data quadlet(s) (in the Trigger Control Register on page 7-16) uses this table to specify several data triggers, each one identifying a quadlet within a

message – including data and trailer quadlets – and compares it with an expected value. The Trigger Channel Number and Trigger Message Number identify the type of message on which to evaluate the trigger. The Trigger Data Index identifies which quadlet's contents are to be looked at where the first quadlet of the message data is at index 0 of the message data. Note that index 0 is the Health Status Word and index 1 is the Heartbeat.

The Trigger Mask is applied to the quadlet contents to isolate important bits in case not all 32 bits are relevant. The Trigger Comparison Value contains the data to which to compare the incoming data and the Trigger Function indicates the type of comparison to be performed (that is, <, >, ==, or !=).

Table 7-40 describes the fields of each entry in the Bus Monitor Data Trigger Table.

Table 7-40: Bus Monitor Data Trigger Table

Word	Description
0	Source channel number
1	Message number
2	Data index (The index is from the beginning of the payload area (that is, 0 is the Health Status Word, 1 is the Heartbeat, 2 is the first message data quadlet, etc.)
3	Function (0 = trigger on data value equals comparison value, 1 = trigger on data value not equal to comparison value, 2 = trigger on data value less than comparison value, 3 = trigger on data value greater than comparison value)
4 – 5	Mask (Each bit set to 1 corresponds to a relevant data bit. Each bit set to 0 corresponds to a "do not care" value)
6 – 7	Comparison value (the value to which the incoming data is to be compared. All comparisons are performed after the mask is applied.)
8	Control Word
9	Status Word

Table 7-41 describes the fields of the Bus Monitor Data Trigger Control Word.

Table 7-41: Bus Monitor Data Trigger Control Word

Bit	Description
01 – 15	Reserved
00	Trigger on (1)/off (0)

Table 7-42 describes the fields of the Bus Monitor Data Trigger Status Word.

Table 7-42: Bus Monitor Data Trigger Status Word

Bit	Description
01 – 15	Reserved
00	Triggered

7.3 Message Area

The Bus Monitor Message Area contains:

- Bus Monitor Receive Stack
- Bus Monitor Linked List
- Banked Window into SDRAM

7.3.1 Bus Monitor Receive Stack

When saving messages to SDRAM, a message stack with 1000 entries describes the last 1000 messages to be saved by the node, allowing you to see, during runtime, a summary of the messages being saved. See Pointer to Beginning of Receive Stack on page 7-12 to obtain the Receive Stack in Dual Port RAM.

Table 7-43 describes the fields of the Bus Monitor Receive Stack.

Table 7-43: Bus Monitor Receive Stack

Word	Description
0	Status
1	Message identifier – sending channel (bits 0 – 6) + message number (bits 7 – 13) + STOF indicator (Bit 15)
2 – 3	1394 Header Word
4 – 6	48-bit Time Tag
7	Reserved

Table 7-44 describes the fields of the Bus Monitor Message Stack Status Word.

Table 7-44: Bus Monitor Message Stack Status Word

Bit	Description
15	Message complete
14	Message in progress
09 – 13	Reserved
08	Vehicle time not progressing
07	STOF timing error (early or late STOF)
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

7.3.2 Bus Monitor Linked List

The 2-MB Dual Port Ram is accessible in real time. The 128-MB SDRAM is accessible only when the Start bit is off and is accessed via Bank Select Register.

You can select to which memory bank the Bus Monitor stores its messages (Dual Port RAM or SDRAM) via the Memory Select Register (page 7-20).

The following pointers are provided for navigating the Linked List:

- Pointer to Most Recent Message on page 7-15
- Pointer to Least Recent Message on page 7-16
- Pointer to Trigger Message on page 7-16
- Pointer to Beginning of Receive Linked List on page 7-12

Note: The Pointer to Beginning of Receive Linked List is only valid when the Linked List is in Dual Port RAM. Otherwise, access the Linked List through the Banked Window. See Banked Window into SDRAM on page 7-31. When the Linked List is stored in SDRAM, the other three pointers are offsets into SDRAM.

Table 7-45 describes the fields in each entry of the bus monitor Linked List structure.

Table 7-45: Bus Monitor Linked List Structure for a General Message

Word	Description
0	Sentinel has four legal values: 1394 (H) indicates a valid general message. (This value is not valid for STOF messages.) 570F (H) indicates a STOF message. (This value is not valid for general messages.) C1C1 (H) indicates no message AAAA (H) indicates time to wrap around to beginning of Linked List Any other value is illegal and probably means that you are not keeping up with the node and there was an overrun.
1	Message Status
2 – 3	Receive Message Counter (number of messages received by node since power-up or node reset)
4 – 6	48-bit Time Tag
7 – 8	Reserved
9	Number of 16-bit words from the sentinel of this message until the next sentinel
2 words	1394 Header Word
8 words	ASM Header
Length based on payload length	Payload
8 words	Packet trailer

Note: The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

Table 7-46 describes the fields in the Receive Message Status Word.

Table 7-46: Receive Message Status Word for a General Message

Bit	Description
15	Message complete
14	Message in progress
13	Matched trigger
12	Header length mismatch (length in 1394 header and payload length in ASM header disagree)
10 – 11	Reserved
09	STOF offset timing error – node transmitted at wrong offset (only if using STOF Offsets Table)
07 – 08	Reserved
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

Table 7-47 describes the fields in each entry of the bus monitor Linked List structure for STOF messages.

Table 7-47: Bus Monitor Linked List Structure for a STOF Message

Word	Description
0	Sentinel has four legal values: 1394 (H) indicates a valid general message. (This value is not valid for STOF messages.) 570F (H) indicates a STOF message. (This value is not valid for general messages.) C1C1 (H) indicates no message AAAA (H) indicates time to wrap around to beginning of Linked List Any other value is illegal and probably means that you are not keeping up with the node and there was an overrun.
1	Message Status
2 – 3	STOF Message Counter (number of STOF messages received by node since power-up or node reset)
4 – 6	48-bit Time Tag
7 – 8	Reserved
9	Number of 16-bit words from the sentinel of this message until the next sentinel
10 – 11	1394 Header Word
12 – 13	CC Branch Status
14 – 15	Network Bus Mode
16 – 17	Vehicle State
18 – 19	Vehicle Time
10 words	STOF TBD data quadlets (see Figure A-1)
2 words	VPC

Note: The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

Table 7-48: Receive Message Status Word for a STOF Message

Bit	Description
15	Message complete
14	Message in progress
09 – 13	Reserved
08	Vehicle time not progressing
07	STOF timing error (early or late STOF)
06	Lost quadlets (Some quadlets that were received on the bus were lost probably due to heavy communications traffic)
05	Reserved
04	Low word count (actual length does not match 1394 header length)
03	Reserved
02	Bad CRC or high word count (actual length does not match 1394 header length)
01	Bad VPC
00	Message error (an error occurred, specified in one of the other bits)

7.3.3 Banked Window into SDRAM

The node supports 128 MB of SDRAM. You can select to use SDRAM via the Memory Select Register on page 7-20. When using SDRAM, you can view 1-MB blocks of SDRAM when the node is stopped via the Bank Select Register. When you activate this register, the node copies the SDRAM to the DPRAM in addresses 100000 (H) to 1FFFFF (H).

You can check which SDRAM bank is currently displayed in the DPRAM window via the Current Bank Register.

For more information, see the Bank Select Register on page 7-20 and the Current Bank Register on page 7-21.

Chapter 8 Mechanical and Electrical Specifications

Chapter 8 describes the mechanical and electrical specifications of the *EXC-1394PCI[e]*. The following topics are covered:

8.1 Board Layout 8-1

8.2 LED Indicators 8-2

8.3 DIP Switches 8-3

8.3.1 Selected ID DIP Switch [SW1] 8-3

8.4 Connectors 8-4

8.4.1 Communications I/O Connector [J1] 8-4

8.4.2 PCI Bus Edge Connector Pinouts 8-8

8.4.3 PCI Express Bus Edge Connector Pinouts 8-10

8.5 Synchronization with External Sources 8-11

8.6 Synchronizing Between EXC-1394PCI[e] Boards 8-12

8.7 Power Requirements 8-12

8.1 Board Layout

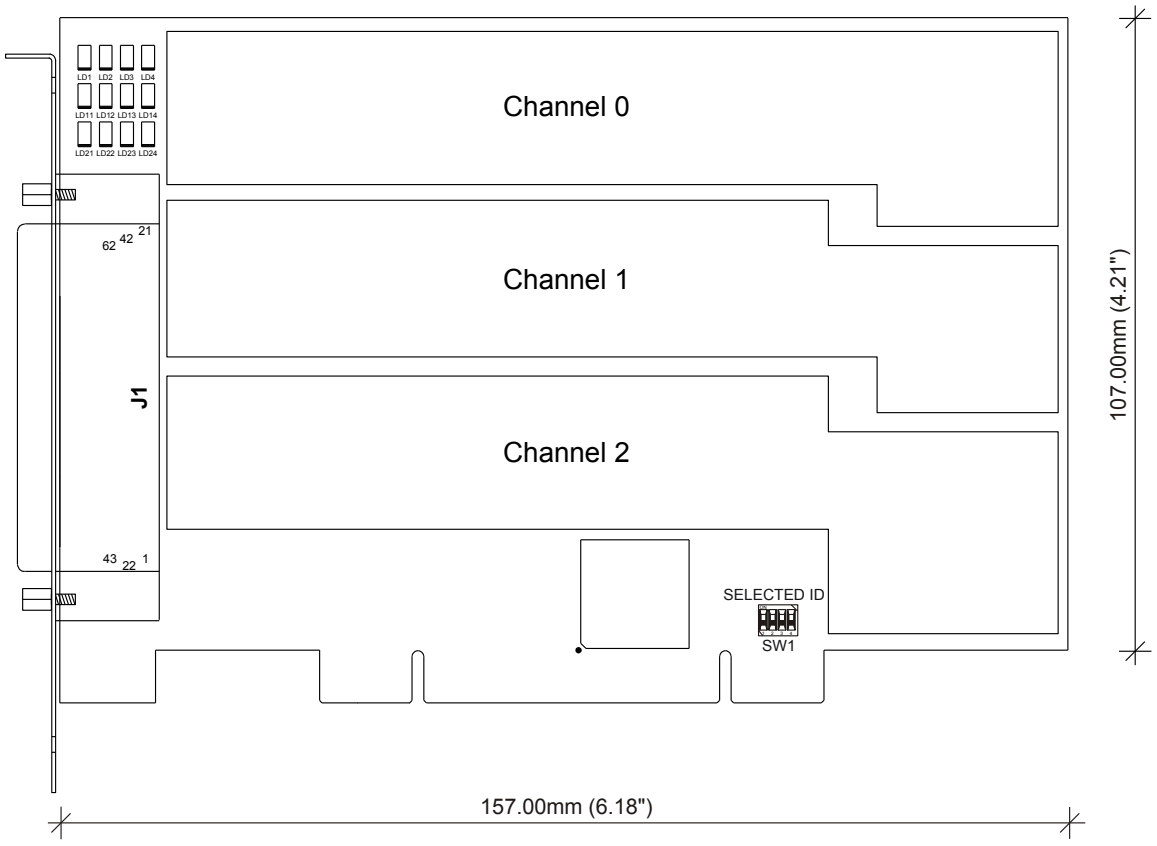

Figure 8-1: *EXC-1394PCI* Board Layout

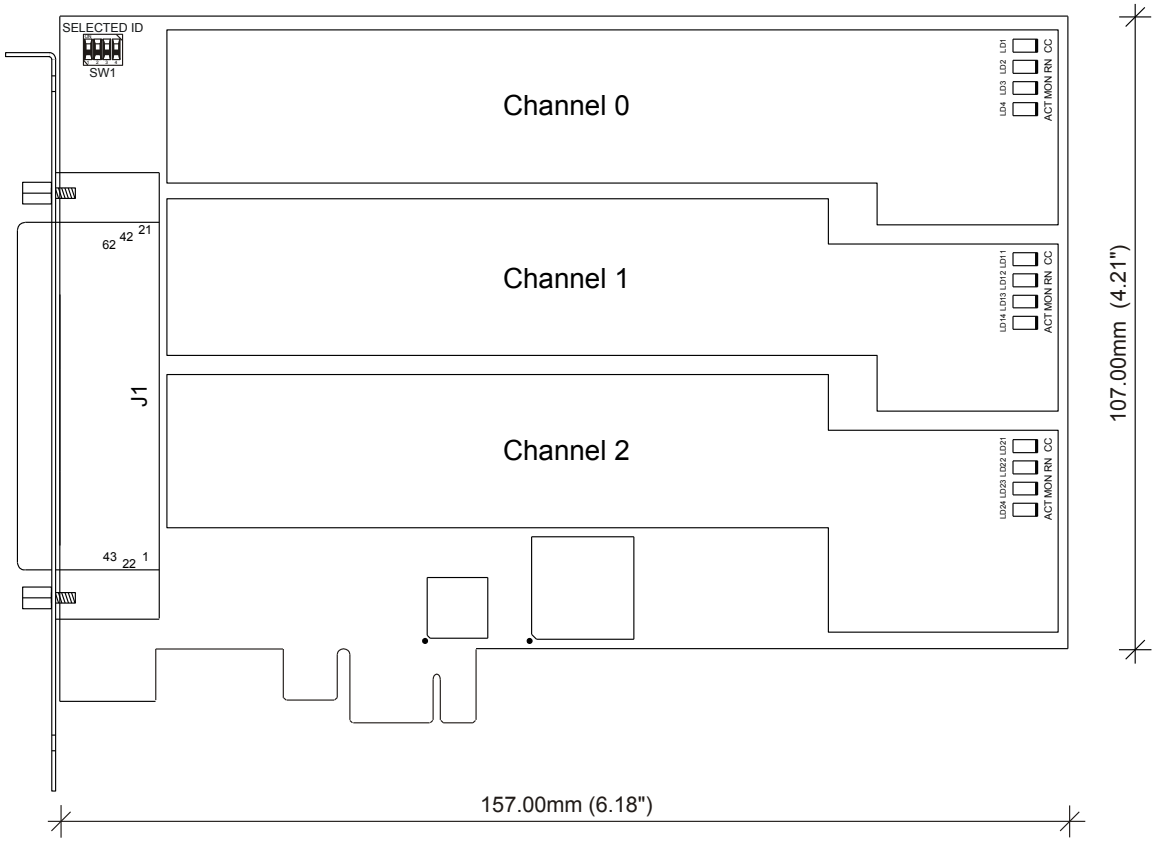

Figure 8-2: *EXC-1394PCIe* Board Layout

8.2 LED Indicators

The *EXC-1394PCI[e]* contains the following LEDs:

Table 8-1: LED Indicators

LED	Name	Color	Indication
LD1	ACT	White	Node 0 Active
LD2	MON	Blue	Node 0 Monitor mode active
LD3	RN	White	Node 0 RN mode active
LD4	CC	Blue	Node 0 CC mode active
LD11	ACT	White	Node 1 Active
LD12	MON	Blue	Node 1 Monitor mode active
LD13	RN	White	Node 1 RN mode active
LD14	CC	Blue	Node 1 CC mode active
LD21	ACT	White	Node 2 Active
LD22	MON	Blue	Node 2 Monitor mode active
LD23	RN	White	Node 2 RN mode active
LD24	CC	Blue	Node 2 CC mode active

8.3 DIP Switches

The *EXC-1394PCI[e]* contains one DIP switch (SW1).

8.3.1 Selected ID DIP Switch [SW1]

This four contact DIP switch provides the board's 'Select ID'. It represents a four bit number of which position #1 is the most significant bit. When a specific bit of the switch is:

- **Off** a value of "1" will be set for that bit
- **On** a value of "0" will be set for that bit

Multiple Board Applications

To provide a unique 'Selected ID', to identify a board by the application software in a multiple board application, the DIP switch should be set differently for each board. For example:

Table 8-2: Dip Switch Settings for Unique 'Selected ID'

Board	ID#1	ID#3
Bit 1	On	On
Bit 2	On	On
Bit 3	On	Off
Bit 4	Off	Off

For multiple board applications, each board's device number may be set by using the Excalibur configuration utility program provided with the drivers, and by setting the 'unique ID' to match that set on the DIP switch shown in Figure 3-5.

Table 8-3: Selected ID Bits

Selected ID	Bit 1	Bit 2	Bit 3	Bit 4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1

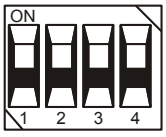

Figure 8-3: DIP Switch SW1 with All Switches Set to ON (Select ID#0)

8.4 Connectors

The *EXC-1394PCI[e]* board contains the following connectors:

- One 62-pin communications I/O connector
- One PCI Bus Edge connector

8.4.1 Communications I/O Connector [J1]

The *EXC-1394PCI[e]* contains all communication I/O signals on one female 62-pin right-angle connectors, J1 (P/N: CONEC 164A20959X). A mating connector (P/N: 163A16629X) and a plastic hood are included. The connector pinouts and signal descriptions are described below.

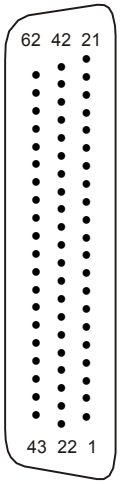

Figure 8-4: Connectors J1 Layout – Front View

Each node's signals are grouped together on the connector. All external signals are contained on connector J1 (except for External Trigger, which is grouped with each node's signals). Pinouts and signal descriptions are listed in Table 8-4 and Table 8-5.

J1 Connector Pinouts

Table 8-4: J1 Connector Pinouts

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	EXTTRSTn	16	0TPA2L	31	SHIELD	47	2TPB1H
2	EXTTCLKI	17	0TPA1H	32	SHIELD	48	2TPB1L
3	2TPA2H	18	0TPA1L	33	SHIELD	49	2TPB0H
4	2TPA2L	19	0TPA0H	34	SHIELD	50	2TPB0L
5	2TPA1H	20	0TPA0L	35	SHIELD	51	1TPB2H
6	2TPA1L	21	N/C	36	SHIELD	52	1TPB2L
7	2TPA0H	22	GND	37	SHIELD	53	1TPB1H
8	2TPA0L	23	IRIGBIN	38	SHIELD	54	1TPB1L
9	1TPA2H	24	SHIELD	39	SHIELD	55	1TPB0H
10	1TPA2L	25	SHIELD	40	SHIELD	56	1TPB0L
11	1TPA1H	26	SHIELD	41	SHIELD	57	0TPB2H
12	1TPA1L	27	SHIELD	42	SHIELD	58	0TPB2L
13	1TPA0H	28	SHIELD	43	EXTTRSOn	59	0TPB1H
14	1TPA0L	29	SHIELD	44	EXTTCLKO	60	0TPB1L
15	0TPA2H	30	SHIELD	45	2TPB2H	61	0TPB1H
				46	2TPB2L	62	0TPB1L

J1 Connector Signal Descriptions

Table 8-5: J1 Connector Signal Descriptions

Pin #	Signal Name	Description
1	EXTTRSTn	External Time Tag Reset TTL Input. Use this low active pulsed signal (minimum 100 nsec wide) to simultaneously reset the Time Tags of all the modules from an external source. Use the signal to synchronize these Time Tags to other boards or systems.[2]
2	EXTTCLKI	External Time Tag Clock TTL Input (Nominal value: 1 MHz). This signal supplies an external global clock for the Time Tags of all the modules. Use the signal to synchronize the Time Tags that are implemented on the modules to other boards or systems. [2] See Time Tag Clock Select Register on page 2-18.
21	N/C	Not Connected
22	GND	Ground
23	IRIGBIN	IRIG B120 Input. IRIG B120 signals have the following specifications: B = 100 pulses per second (PPS), 10 msec count 1 = Sine wave carrier, amplitude modulated 2 = 1 kHz carrier wave (1 msec resolution) 0 = Binary Coded Decimal (BCD), Control Functions (CF) depending on the user application, Straight Binary Second (SBS) of day (0 – 86400)
24	SHIELD	
43	EXTTRSOn	External Time Tag Reset TTL Output. This low active signal is activated each time a Global Time Tag Reset is applied. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules. This signal is activated by either the internal Global Time Tag signal (see Software Reset Register on page 2-16) or from the External Time Tag signal (EXTTRSTn). [2]
44	EXTTCLKO	External Time Tag Clock TTL Output (1 MHz). This signal is the Global Clock that is supplied to all the modules for their Time Tags. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules. The source of this clock is either the External Time Tag Clock EXTTCLKI or the Internal Time Tag Clock. See Time Tag Clock Select Register on page 2-18.

[2] See Synchronization with External Sources on page 8-11 and Synchronizing Between EXC-1394PCI[e] Boards on page 8-12.

Pin #	Signal Name	Description	
3, 4	2TPA2H/2TPA2L	Rx+/Rx-	
25, 26		Reference Shield	Node 2 Port 2 - 1394B
45, 46	2TPB2H/2TPB2L	Tx+/Tx-	
5, 6	2TPA1H/2TPA1L	Rx+/Rx-	
27, 28		Reference Shield	Node 2 Port 1 - 1394B
47, 48	2TPB1H/2TPB1L	Tx+/Tx-	
7, 8	2TPA0H/2TPA0L	Rx+/Rx-	
29, 30		Reference Shield	Node 2 Port 0 - 1394B
49, 50	2TPB0H/2TPB0L	Tx+/Tx-	
9, 10	1TPA2H/1TPA2L	Rx+/Rx-	
31, 32		Reference Shield	Node 1 Port 2 - 1394B
51, 52	1TPB2H/1TPB2L	Tx+/Tx-	
11, 12	1TPA1H/1TPA1L	Rx+/Rx-	
33, 34		Reference Shield	Node 1 Port 1 - 1394B
53, 54	1TPB1H/1TPB1L	Tx+/Tx-	
13, 14	1TPA0H/1TPA0L	Rx+/Rx-	
35, 36		Reference Shield	Node 1 Port 0 - 1394B
55, 56	1TPB0H/1TPB0L	Tx+/Tx-	
15, 16	0TPA2H/0TPA2L	Rx+/Rx-	
37, 38		Reference Shield	Node 0 Port 2 - 1394B
57, 58	0TPB2H/0TPB2L	Tx+/Tx-	
17, 18	0TPA1H/0TPA1L	Rx+/Rx-	
39, 40		Reference Shield	Node 0 Port 1 - 1394B
59, 60	0TPB1H/0TPB1L	Tx+/Tx-	
19, 20	0TPA0H/0TPA0L	Rx+/Rx-	
41, 42		Reference Shield	Node 0 Port 0 - 1394B
61, 62	0TPB0H/0TPB0L	Tx+/Tx-	

8.4.2 PCI Bus Edge Connector Pinouts

Table 8-6: PCI Bus Edge Connector Pinouts

Pin #	Signal Name	Pin #	Signal Name
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GROUND	A3	TMS
B4	TDO	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V
B9	PRSNT1#	A9	RESERVED
B10	RESERVED	A10	+5V
B11	PRSNT2#	A11	RESERVED
B12 B13	CONNECTOR KEY	A12 A13	CONNECTOR KEY
B14	RESERVED	A14	RESERVED
B15	GROUND	A15	RST#
B16	CLK	A16	+5V
B17	GROUND	A17	GNT#
B18	REQ#	A18	GROUND
B19	+5V (I/O)	A19	RESERVED
B20	AD[31]	A20	AD[30]
B21	AD[29]	A21	+3.3V
B22	GROUND	A22	AD[28]
B23	AD[27]	A23	AD[26]
B24	AD[25]	A24	GROUND
B25	+3.3V	A25	AD[24]
B26	C/BE[3]#	A26	IDSEL
B27	AD[23]	A27	+3.3V
B28	GROUND	A28	AD[22]
B29	AD[21]	A29	AD[20]
B30	AD[19]	A30	GROUND
B31	+3.3V	A31	AD[18]
B32	AD[17]	A32	AD[16]
B33	C/BE[2]#	A33	+3.3V
B34	GROUND	A34	FRAME#
B35	IRDY#	A35	GROUND
B36	+3.3V	A36	TRDY#

Pin #	Signal Name	Pin #	Signal Name
B37	DEVSEL#	A37	GROUND
B38	GROUND	A38	STOP#
B39	LOCK#	A39	+3.3V
B40	PERR#	A40	SDONE
B41	+3.3V	A41	SBO#
B42	SERR#	A42	GROUND
B43	+3.3v	A43	PAR
B44	C/BE[1]#	A44	AD[15]
B45	AD[14]	A45	+3.3V
B46	GROUND	A46	AD[13]
B47	AD[12]	A47	AD[11]
B48	AD[10]	A48	GROUND
B49	GROUND	A49	AD[09]
B50 B51	CONNECTOR KEY	A50 A51	CONNECTOR KEY
B52	AD[08]	A52	C/BE[0]#
B53	AD[07]	A53	+3.3V
B54	+3.3V	A54	AD[06]
B55	AD[05]	A55	AD[04]
B56	AD[03]	A56	GROUND
B57	GROUND	A57	AD[02]
B58	AD[01]	A58	AD[00]
B59	+5V (I/O)	A59	+5V
B60	ACK64#	A60	REQ64#
B61	+5V	A61	+5V
B62	+5V	A62	+5V

8.4.3 PCI Express Bus Edge Connector Pinouts

Table 8-7: PCI Express Bus Edge Connector Pinouts

Side B Connector			Side A Connector	
Pin #	**Signal Name**	**Description**	**Signal Name**	**Description**
1	+12V	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12V	+12 volt power	+12V	+12 volt power
3	RSVD	Reserved	+12V	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3V	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3V	+3.3 volt power
10	3.3Vaux	3.3 volt auxiliary power	+3.3V	+3.3 volt power
11	WAKE#	Link reactivation	PWRGD	Power good
		MECHANICAL KEY		
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock, differential pair
14	HSOp	Transmitter lane, differential pair	REFCLK-	
15	HSOn		GND	Ground
16	GND	Ground	HSIp	Receiver lane, differential pair
17	PRSNT#2	Hot plug detect	HSIn	
18	GND	Ground	GND	Ground

8.5 Synchronization with External Sources

To synchronize an *EXC-1394PCI[e]* board to an external system, the external clock source and the external reset must be connected to the EXTTCLKI and the EXTTRSTn signals respectively.

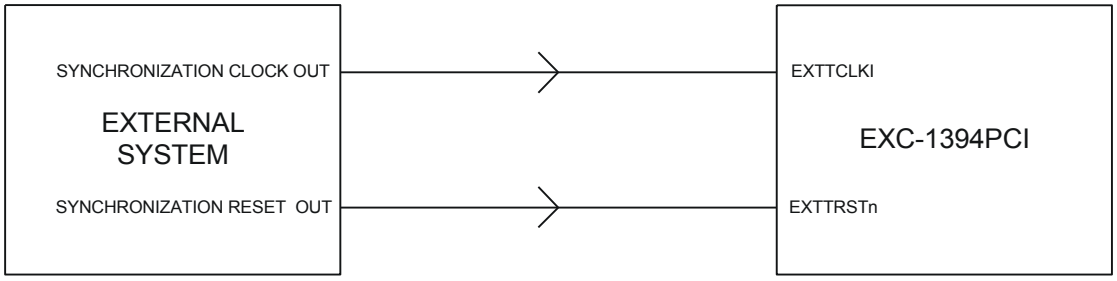

Figure 8-5: Synchronization of an *EXC-1394PCI[e]* Board to an External System

To synchronize an external system to an *EXC-1394PCI[e]* board, the EXTTCLKO and the EXTTRSOn signals need to be connected to the external clock source and the external reset respectively.

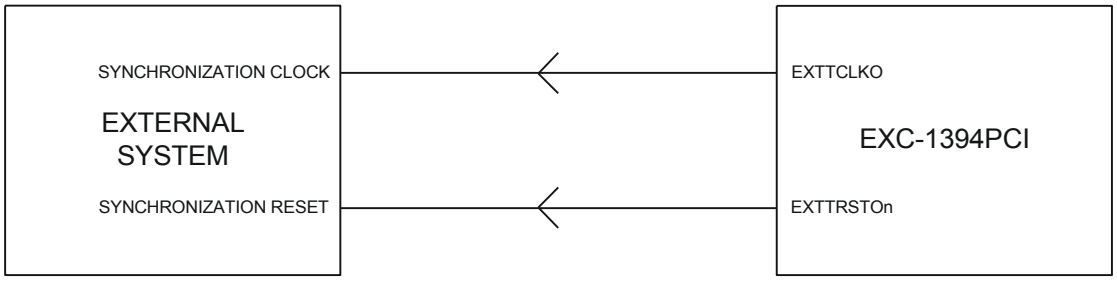

Figure 8-6: Synchronization of an External System to an *EXC-1394PCI[e]* Board

Note: The synchronization clock and reset signals may be connected to multiple targets to achieve system wide synchronization.

8.6 Synchronizing Between EXC-1394PCI[e] Boards

To synchronize multiple *EXC-1394PCI[e]* boards the EXTTCLKO and the EXTTRSOn signals of one board need to be connected to all the EXTTCLKI and the EXTTRSTn signals respectively, of the remaining boards.

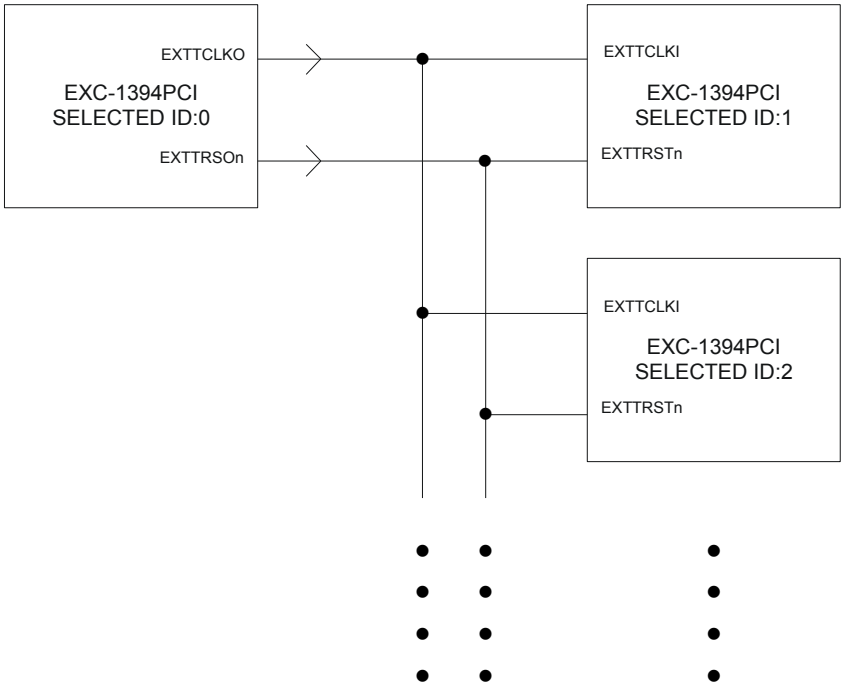

Figure 8-7: Synchronization Between *EXC-1394PCI[e]* Boards

8.7 Power Requirements

The typical power requirements for the *EXC-1394PCI* and *EXC-1394PCIe* boards are as follows:

For PCI: 1.8A @ 5V

For PCI Express: 2.1A @ 3.3V

Chapter 9 Ordering Information

Chapter 9 explains which options to indicate when ordering the *EXC-1394PCI[e]* board:

Table 9-1: Ordering Information

Basic Part #	Option	Description
EXC-1394PCI-*x*		The *EXC-1394PCI* is a 1394 PCI interface board with up to four nodes. Supports CC, RN, Asynchronous and Bus Monitor modes. **Note: '*x*'** indicates the number of nodes required (1 – 3).
EXC-1394PCIe-*x*		The *EXC-1394PCIe* is a 1394 PCI Express interface board with up to four nodes. Supports CC, RN, Asynchronous and Bus Monitor modes. **Note: '*x*'** indicates the number of nodes required (1 – 3).
	-E	Extended temperature board (-40° – +85°)
	-001	With conformal coating

Appendix A 1394 Message Formats

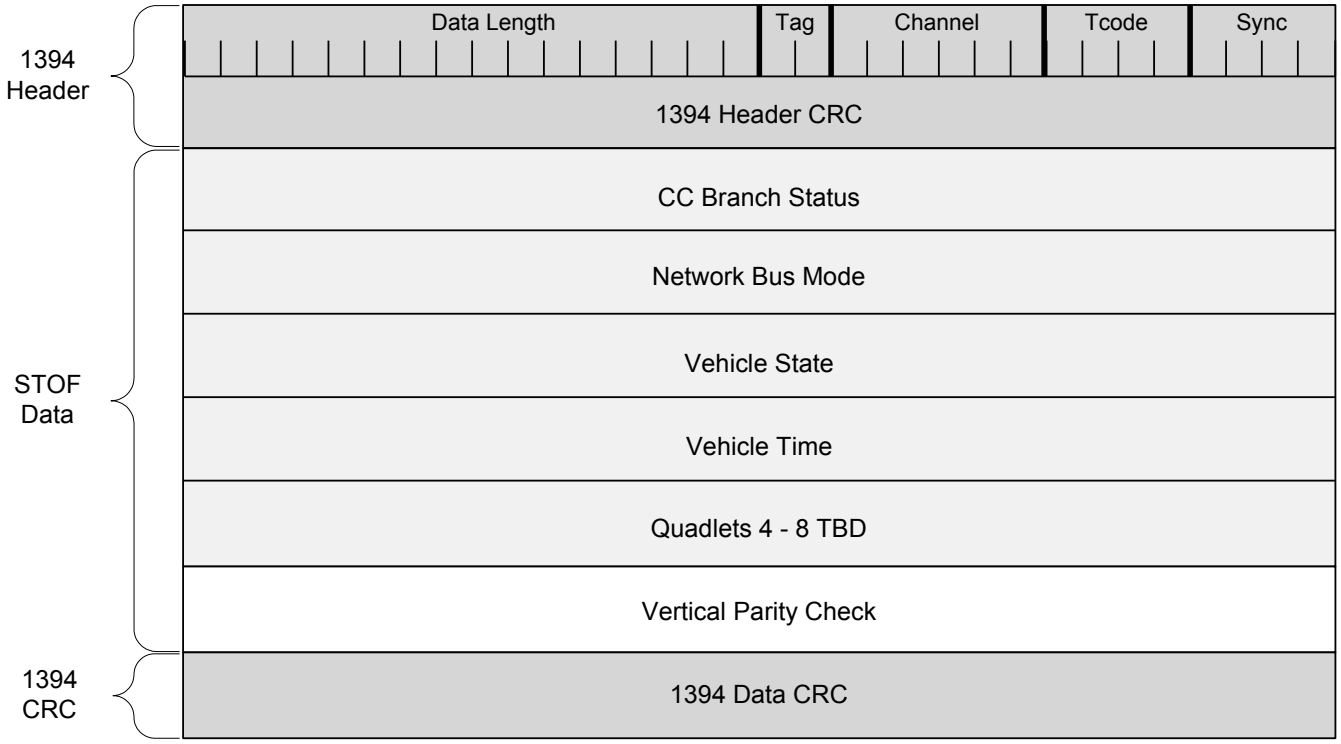

Figure A-1: STOF Packet Format

Note:

- The Vehicle Time is specified in increments of 25 μsec.
- The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

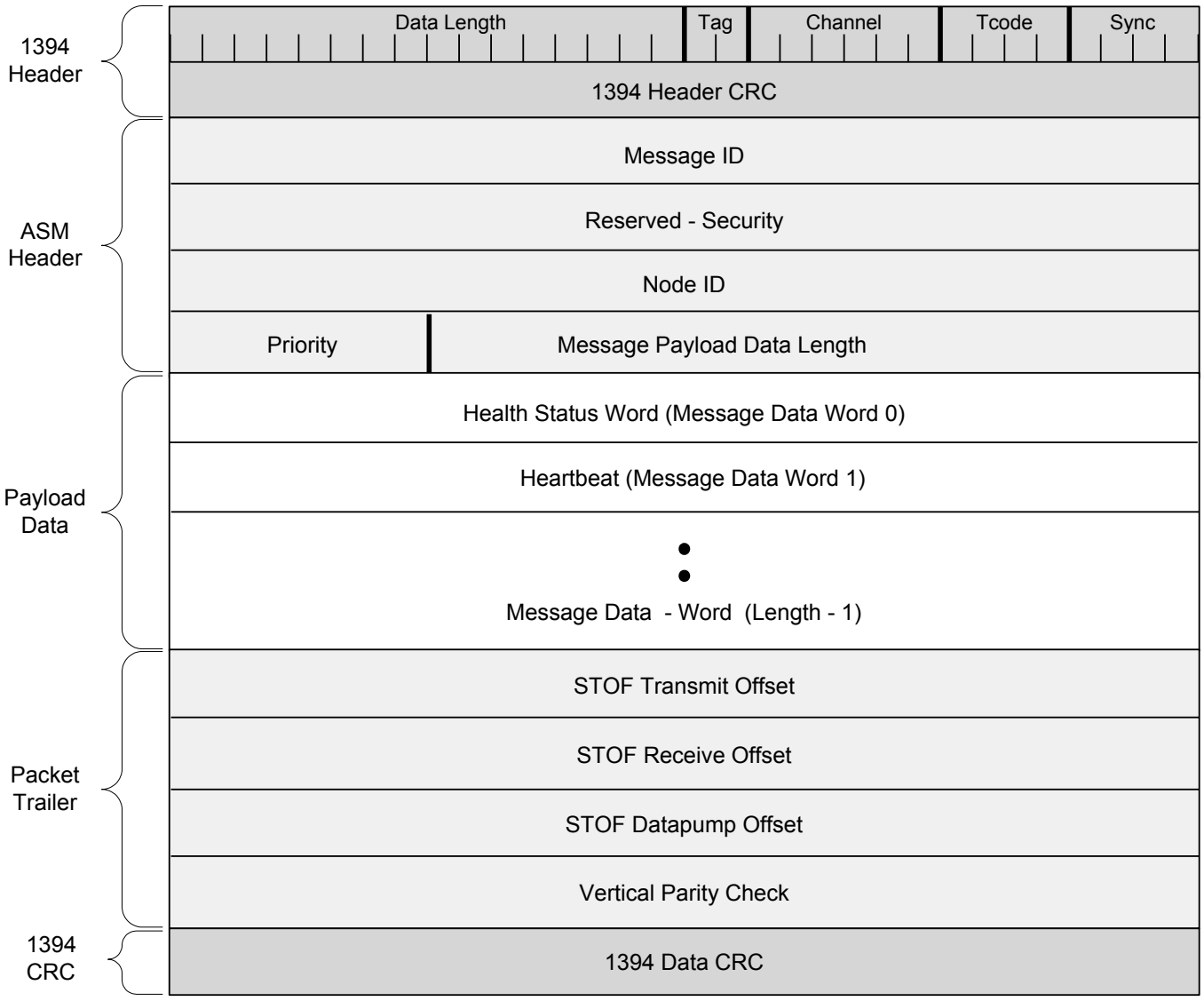

Figure A-2: Asychronous Data Packet Format

Figure A-2 shows the complete data packet transmitted/received in CC, RN and Bus Monitor modes. For Transmit Messages, this includes parts that are supplied by the user and by the firmware. For the parts that are supplied by the user, see Figure 4-1 on page 4-19 and Figure 5-1 on page 5-20. For Asynchronous mode messages, see Figure 6-1 on page 6-13.

Note:

- The *EXC-1394PCI[e]* board's Message ID is a 32-bit number represented as an unsigned long integer. It is a decimal number. The lowest two digits represent the message number from 00 – 99, for a total of 100 messages per channel. The next two digits represent the channel number (0 – 63). The rest of the Message ID, usually representing the CC branch, is ignored by the node.
- The 1394 Header CRC and 1394 Data CRC are stripped from the packet and are not stored by the node.

The information contained in this document is believed to be accurate. However, no responsibility is assumed by Excalibur Systems, Inc. for its use and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

November 2015, Rev A-8